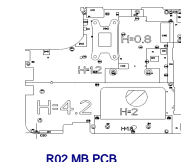


# R02A DIS SYSTEM DIAGRAM



+CPU_VCORE(MAX17811)	Page 43
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+1.1V_SUS(RT8209A)	Page 40
+1.2V_RUN(RT8209A)	Page 44
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Charger	

**SODIMMO**  
Max. 4GB  
Page 12

Dual Channel  
1333Mhz  
DDR3  
Channel A

**SODIMM1**  
Max. 4GB  
Page 13

Dual Channel  
1333Mhz  
DDR3  
Channel B

**AMD**  
35W  
Socket FS1-Llano  
APU ( CPU + GPU )  
uPGA 722 pin

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Travis LVDS

**LVDS**  
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P\_GFX[8:15] **ATI GPU**  
Seymour XT 15W  
(M2 package)  
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**VRAM**  
DDR3 1G  
(128Mx16\*4)  
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10/100  
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IO Board

**WLAN**  
WiFi+BT3.0  
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PCI-E

UMI

DP1

DP to VGA

DP1\_VGA

**VGA**  
Page 24

VGA Board

**AMD**  
FCH  
Hudson-M3  
FCBGA 656 pin

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USB 2.0 **SPI ROM**  
4M Byte  
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**Card Reader**  
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**Webcam**  
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USB 3.0 & USB 2.0

**USB 3.0 Re-driver**  
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**USB3.0&2.0 Combo port**  
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IO Board

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Page 35

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HOTKEY Board

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TP Board

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IO Board

LPC

Azalia

**AUDIO CODEC**  
ALC269Q-VB6-GR  
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**Speaker 2W**  
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IO Board

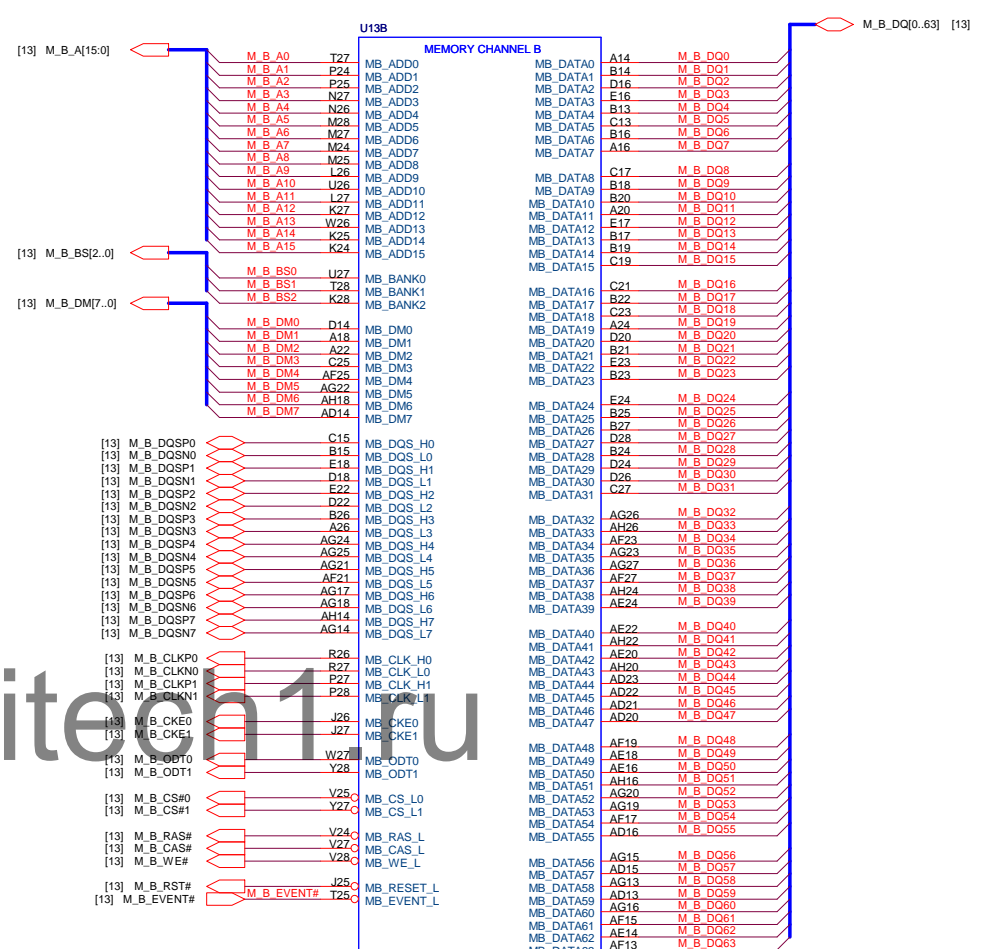
**HP/MIC**

**Analog MIC**

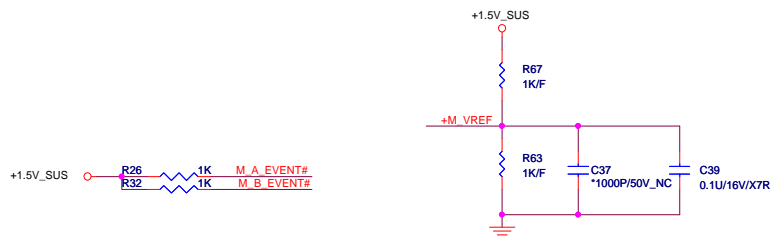




6090030200G\_FS1\_APU



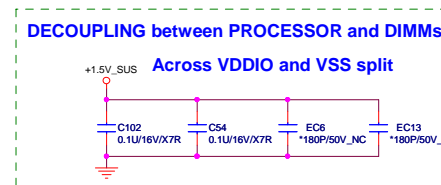
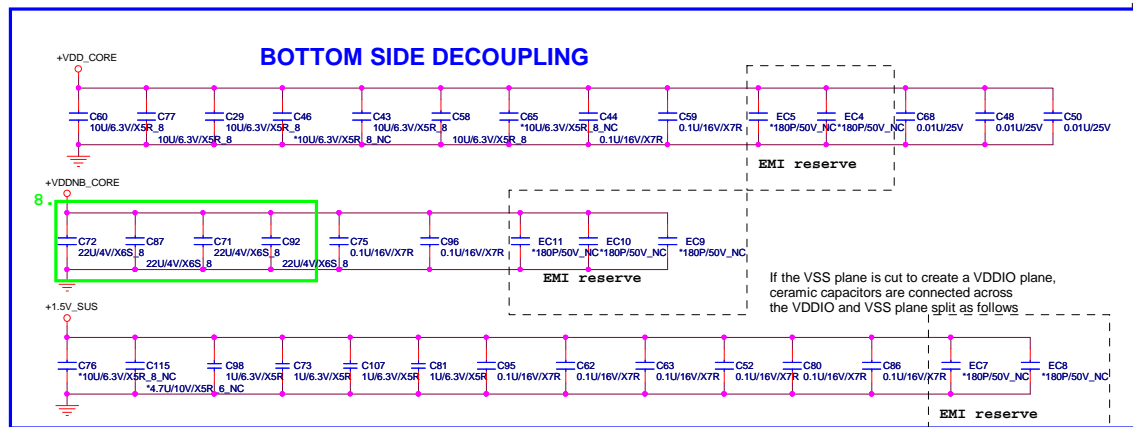
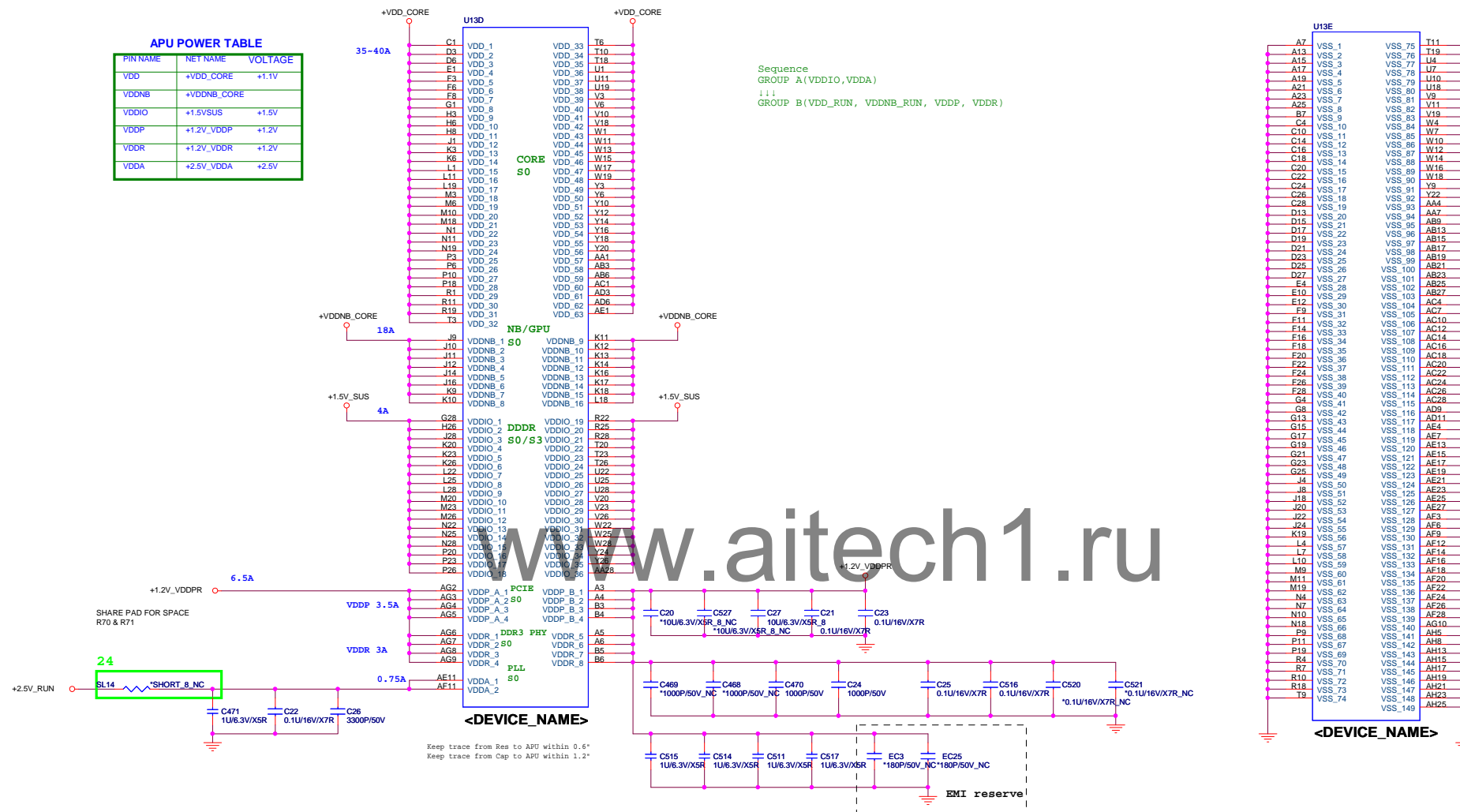
6090030200G\_FS1\_APU



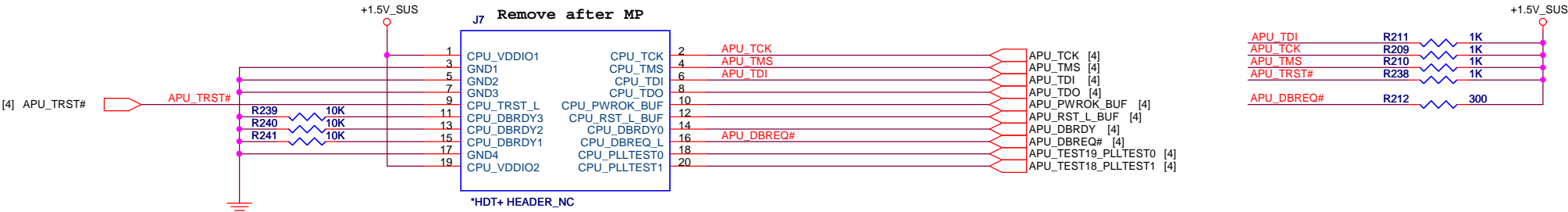
Quanta Computer Inc.  
PROJECT : R02A



PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

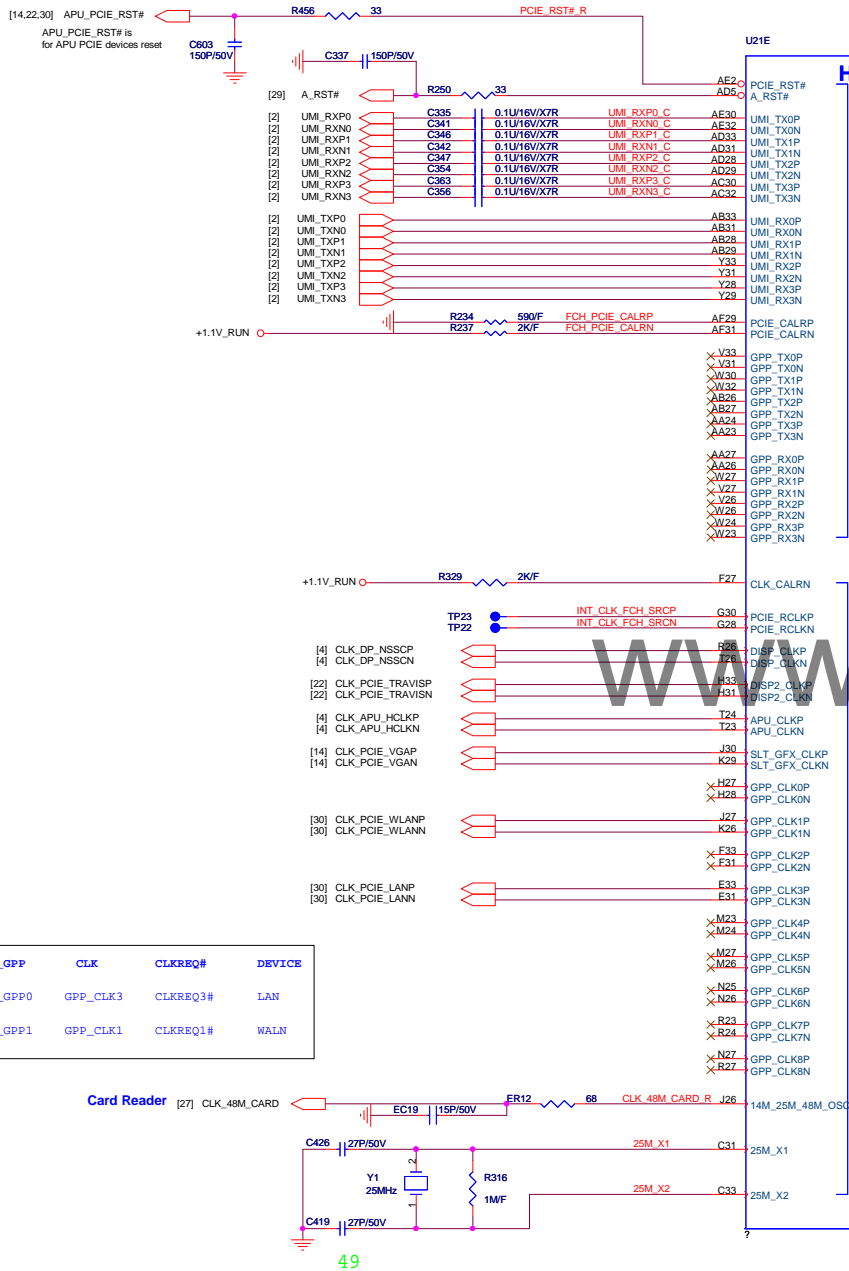


HDT+ Connector    Debug only



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## HUDSON-M2

Part 1 of 5

PCIE RST# R

PCIE\_RST# R

PCIE\_RST# R

PCIE\_RST# R

PCIE\_RST# R

PCIE\_RST# R

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PCIE\_RST# R

PCIE\_RST# R

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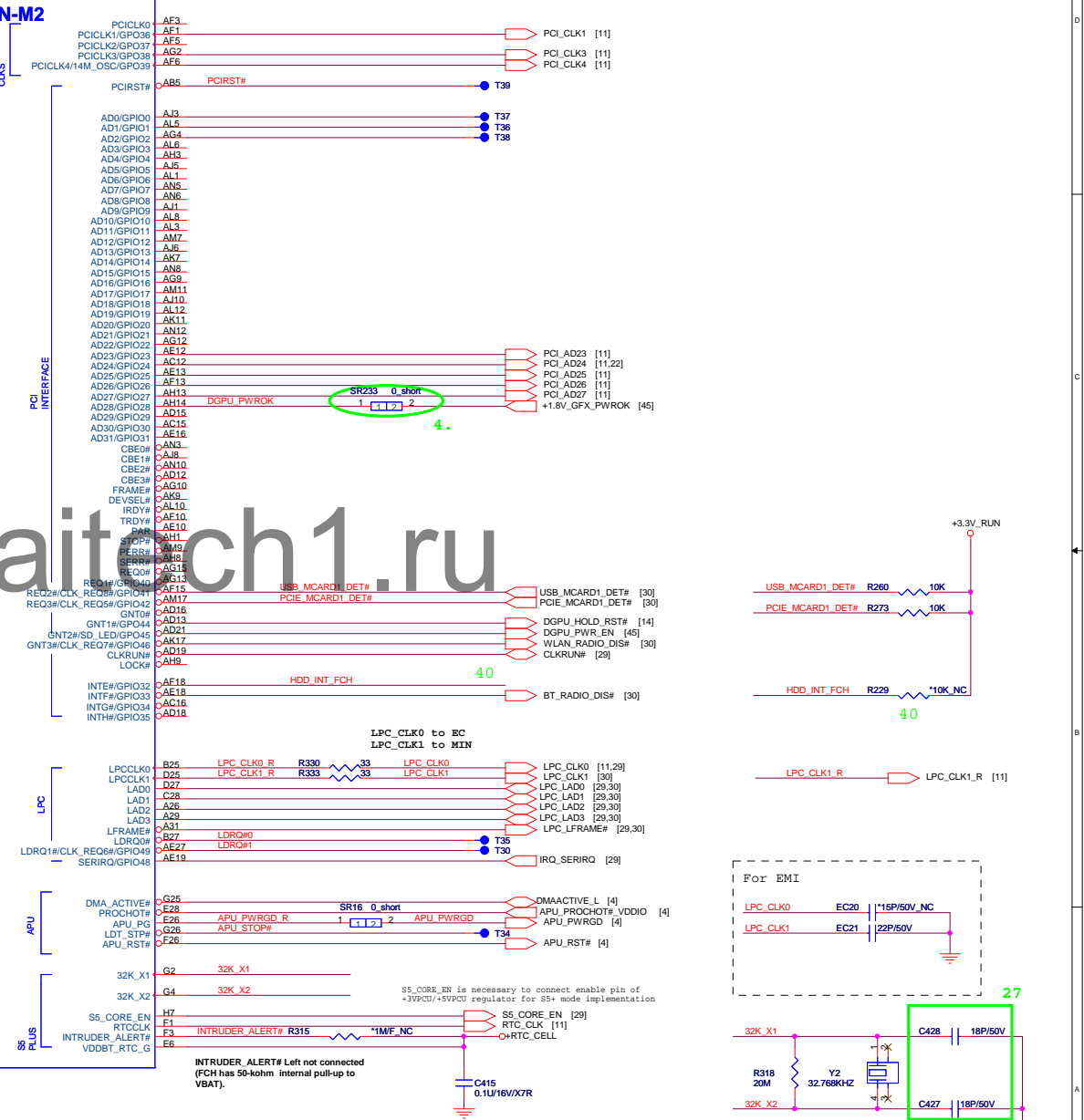
PCIE\_RST# R

PCIE\_RST# R

PCIE\_RST# R

PCIE\_RST# R

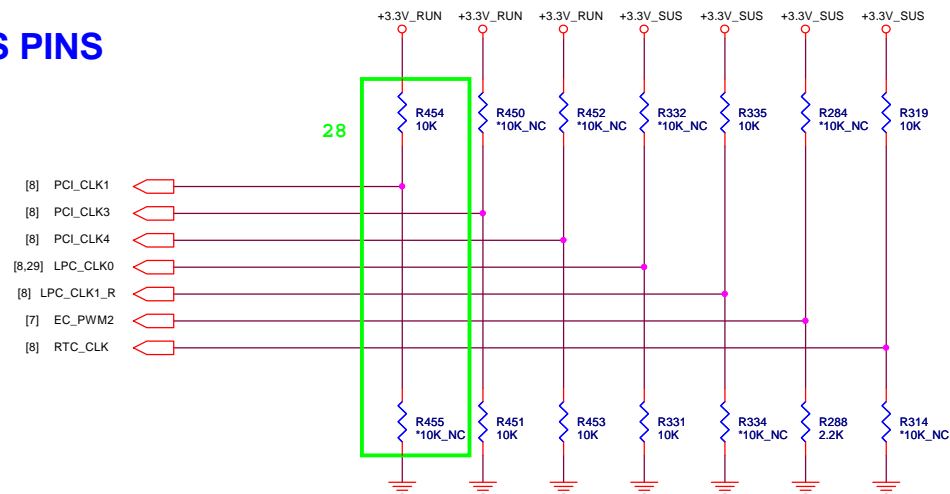
PCIE\_RST# R







STRAPS PINS

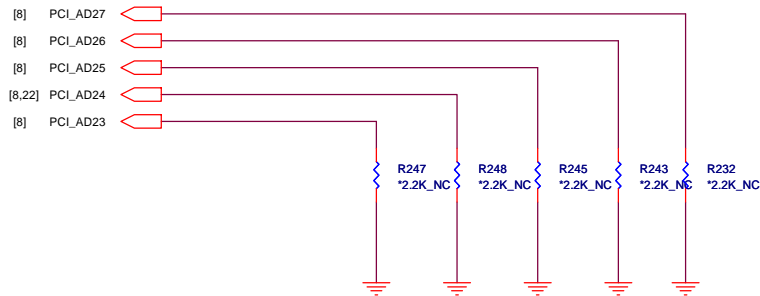


REQUIRED STRAPS

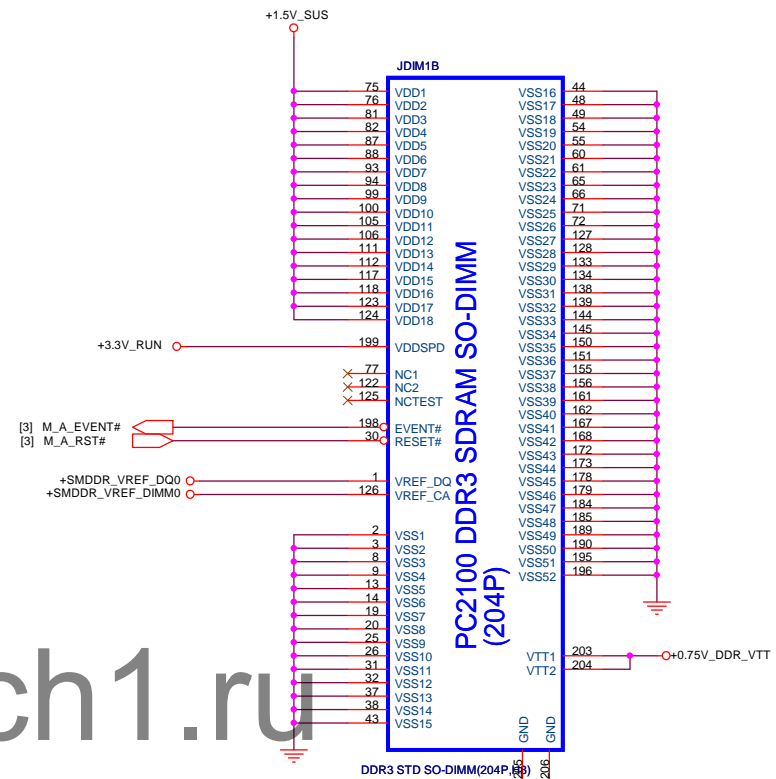
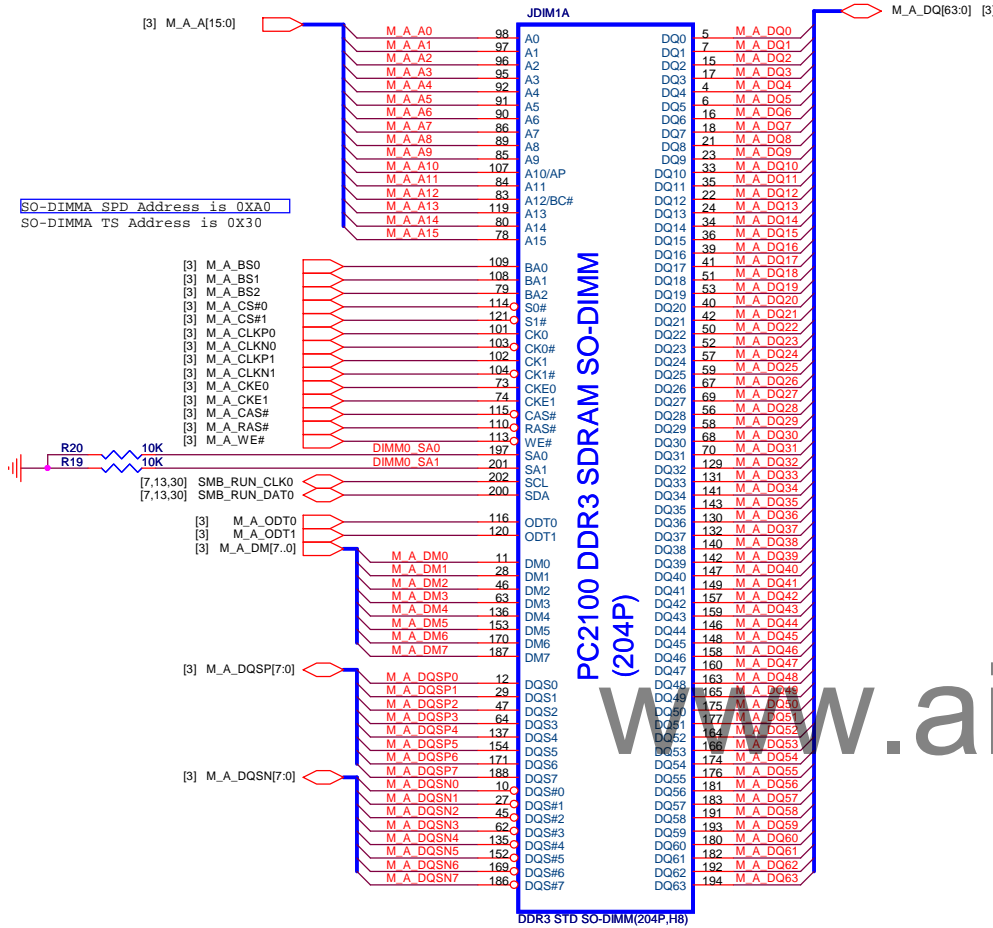
	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1_R	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED	LPC ROM	S5 PLUS MODE DISABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

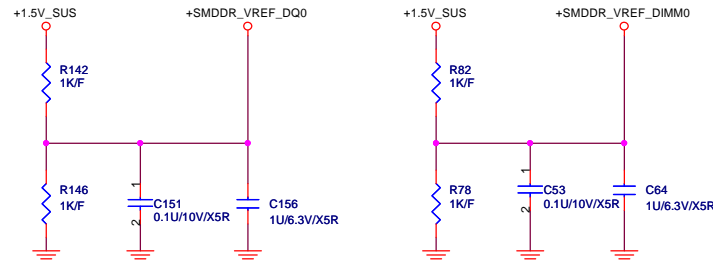
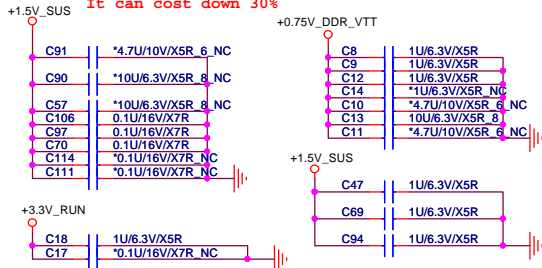


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

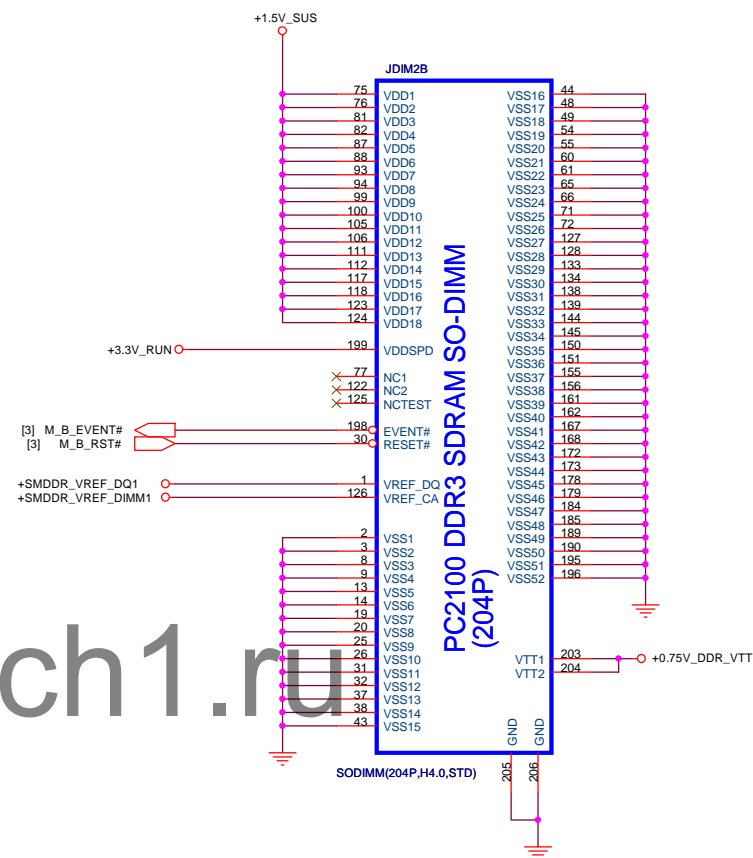
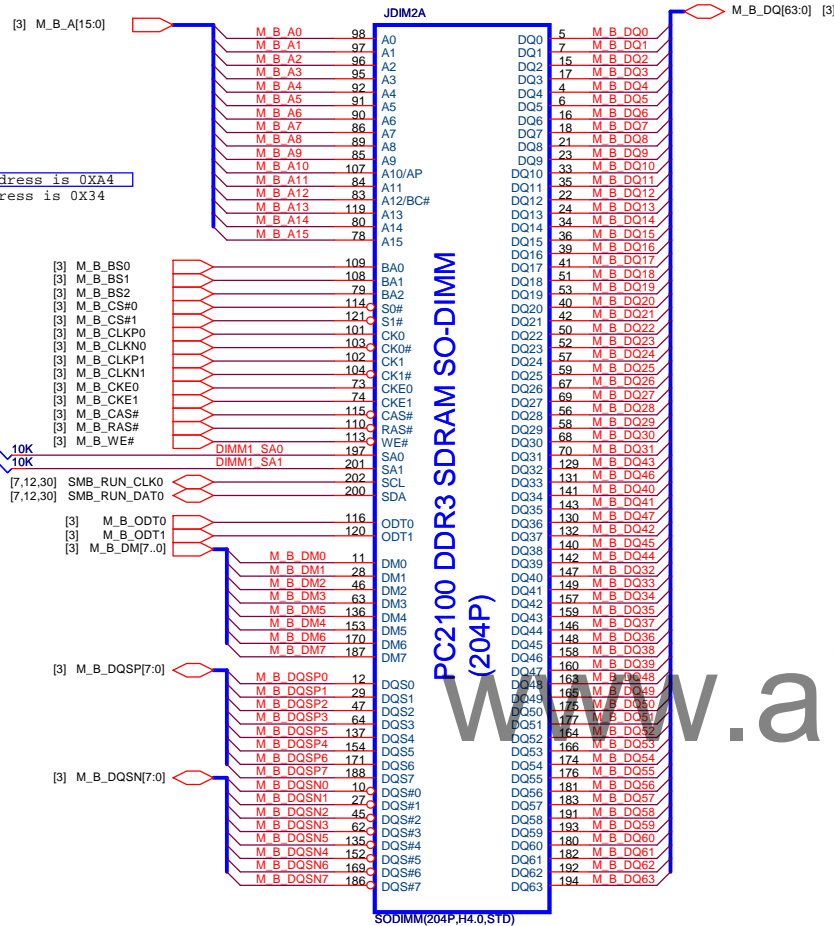


### Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603  
It can cost down 30%

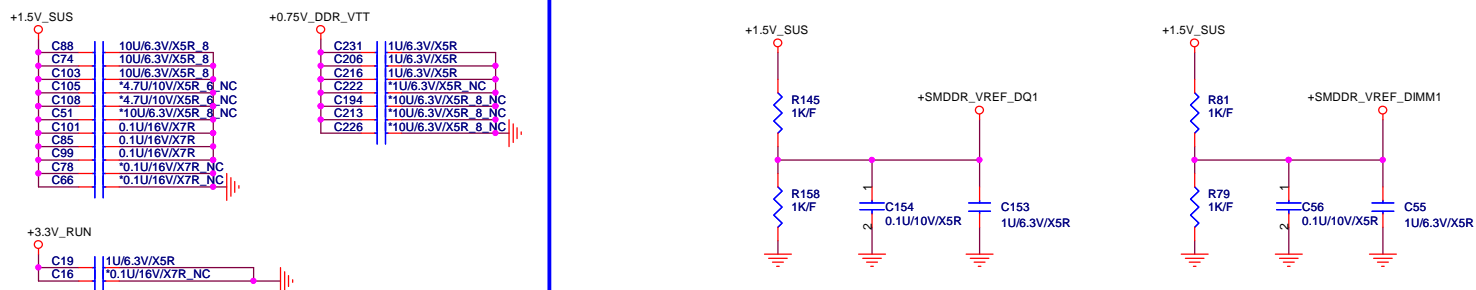


**Quanta Computer Inc.**  
**PROJECT : R02A**



### Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603  
It can cost down 30%

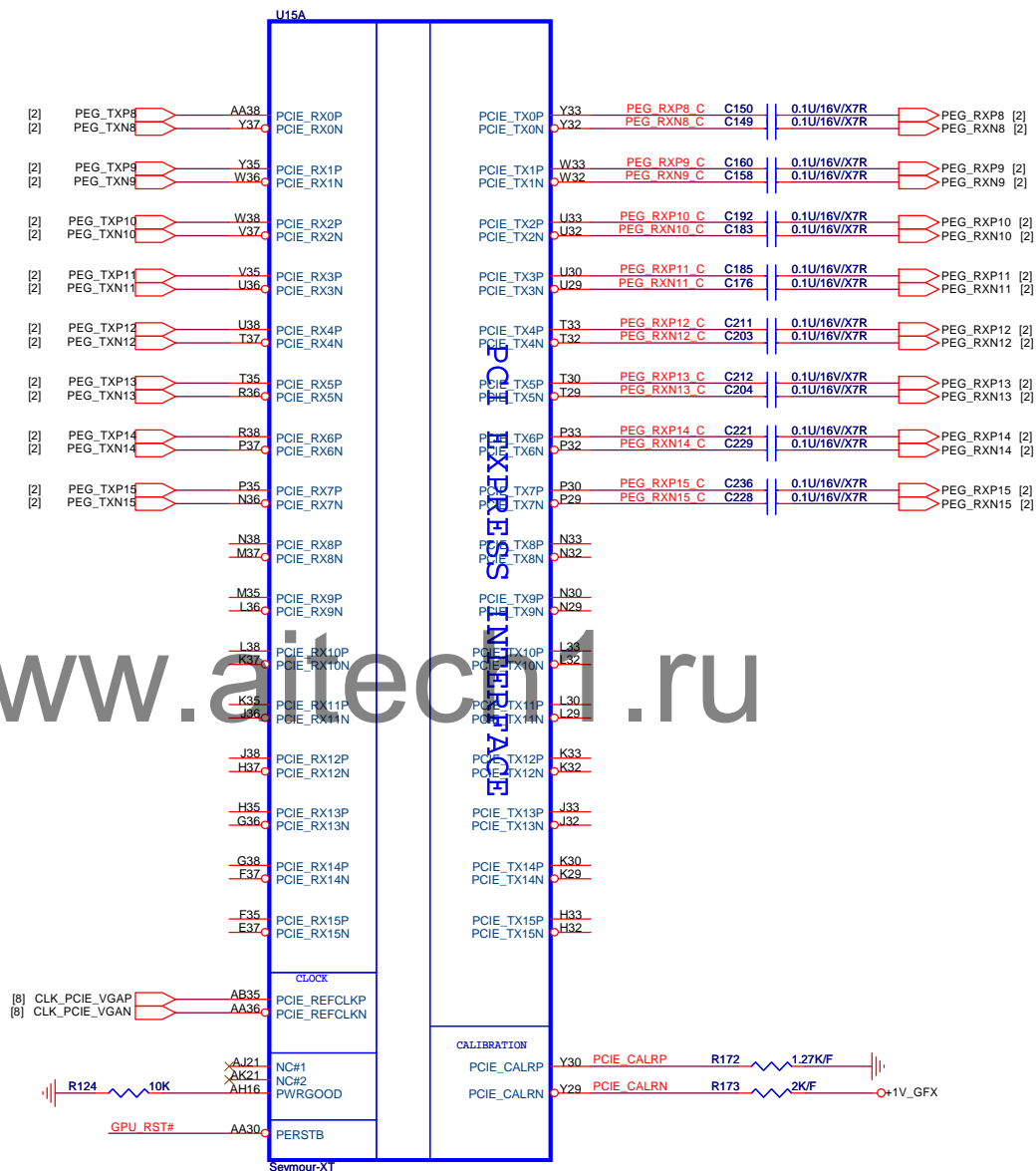
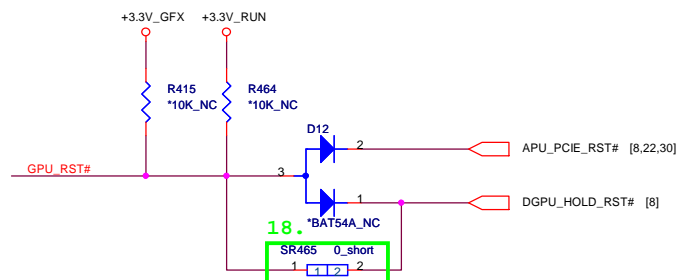


**Quanta Computer Inc.**

**PROJECT : R02A**

Size	Document Number	Rev
	<b>DDR3 DIMM-1</b>	2B
Date:	Thursday, June 30, 2011	Sheet 13 of 47

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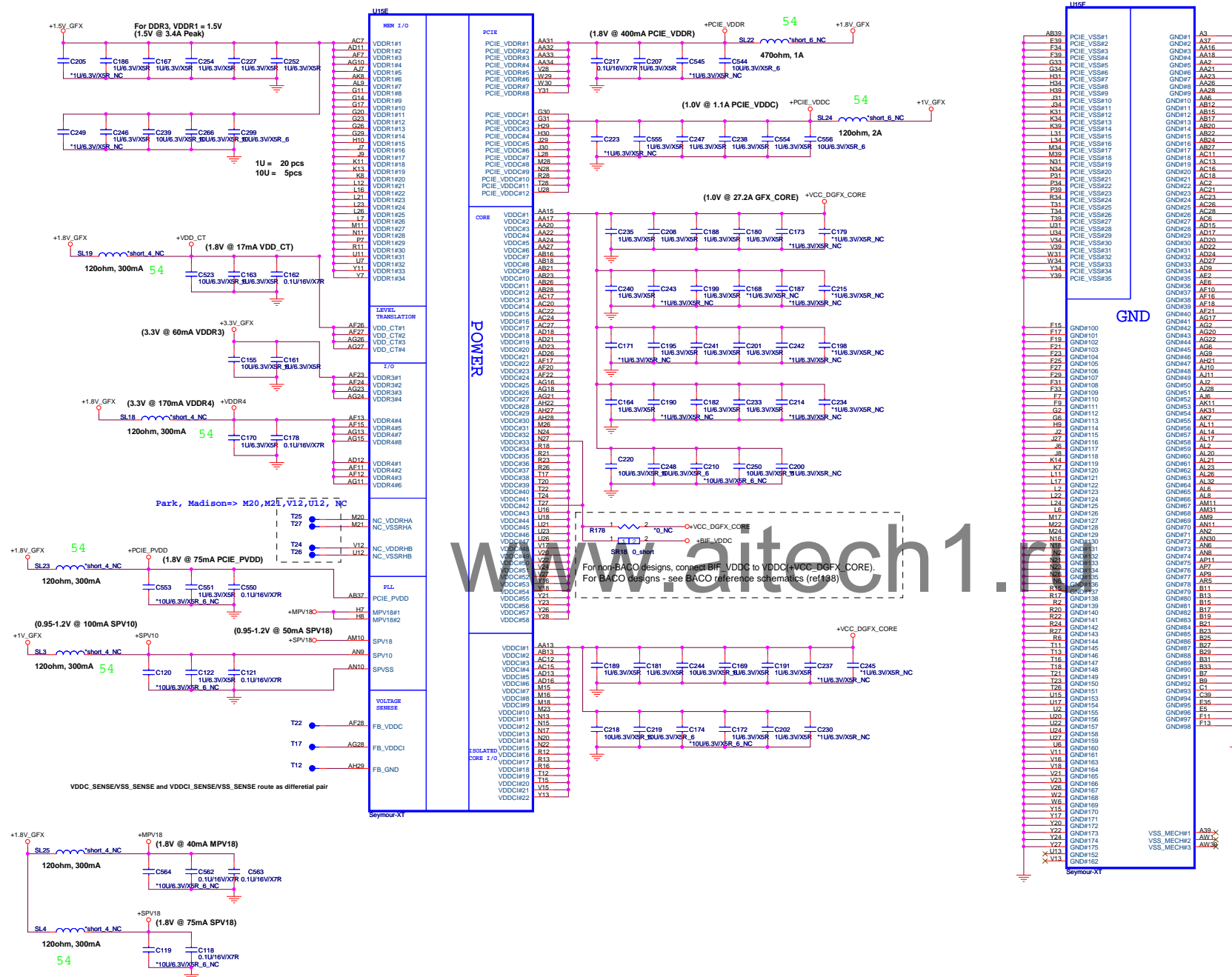


Quanta Computer Inc.

PROJECT : R02A





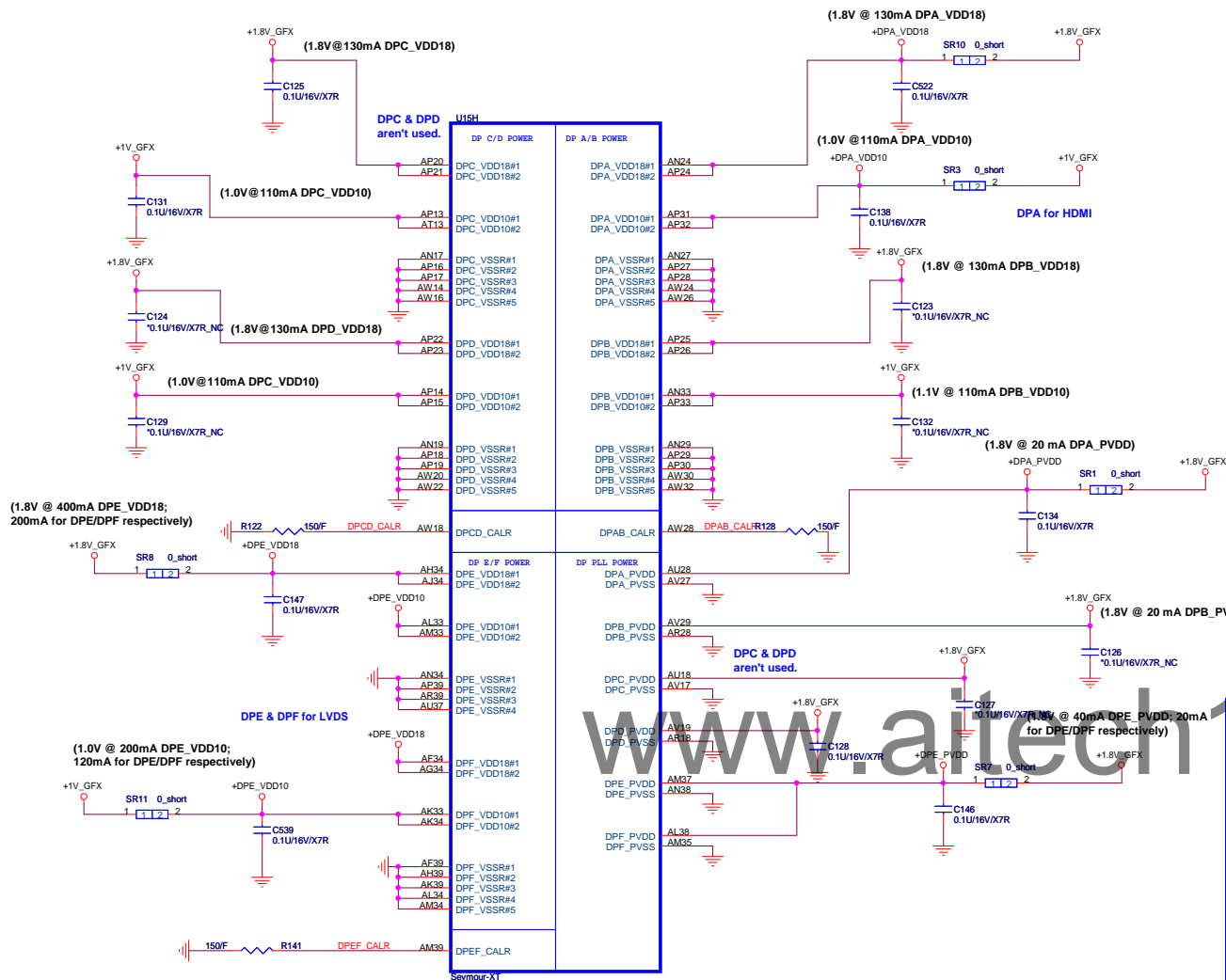


PowerXpress control signal for Madsion and Park only  
If not used, can be disconnected. (AL21 pin)

PX\_EN = LOW, turn on  
PX\_EN = HIGH, turn off

**Reserve for support BACO mode**

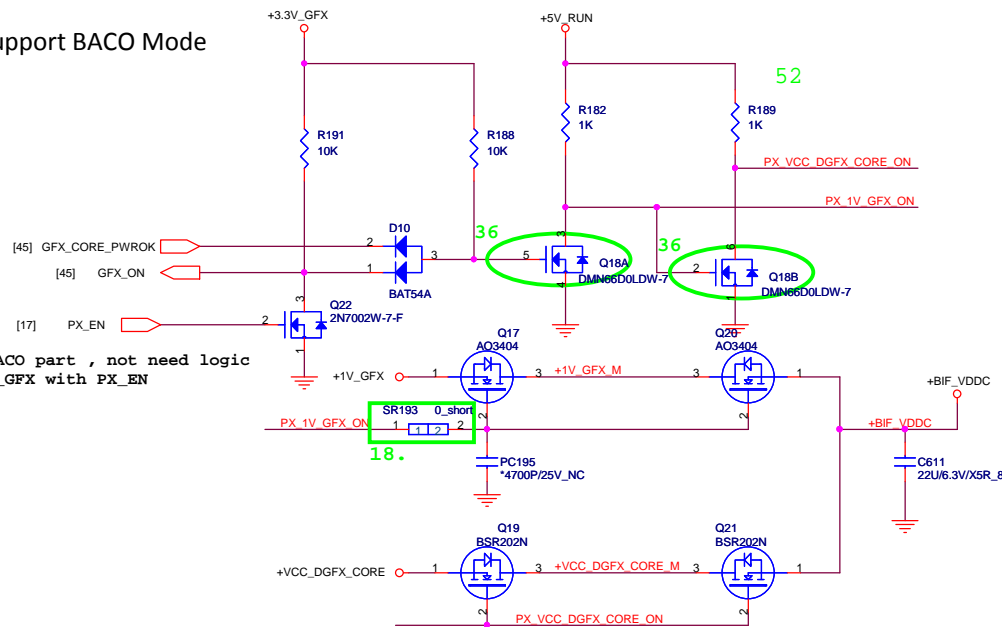
AL21 For PX\_EN, refer to the BACO reference schematics for detail



- ### GPU Power Rail List
- |                     |                       |
|---------------------|-----------------------|
| <b>+1V_GFX=&gt;</b> | <b>+1.8V_GPU=&gt;</b> |
| +DPA_VDD10          | +A2VDDQ               |
| +SPV10              | +AVDD                 |
| +DPE_VDD10          | +DPA_PVDD             |
| +DPLL_VDDC          | +DPA_VDD18            |
| +PCIE_VDDC          | +DPE_PVDD             |
|                     | +DPE_VDD18            |
|                     | +DPLL_PVDD            |
|                     | +MPV18                |
|                     | +PCIE_PVDD            |
|                     | +PCIE_VDDR            |
|                     | +SPV18                |
|                     | +TSVDD                |
|                     | +VDD1DI               |
|                     | +VDD2DI               |
|                     | +VDD_CT               |
|                     | +VDDR4                |

- ### GPU Power-on sequence
- 1 => +3V\_GFX
  - 2 => +VCC\_DGFX\_CORE
  - 3 => +1V\_GFX
  - 4 => +1.5V\_GFX
  - 5 => +1.8V\_GFX
  - 6 => dGPU\_PWROK

## Support BACO Mode



GFX\_ON=1, for Normal Operation (Default)  
GFX\_ON=0, for BACO MODE

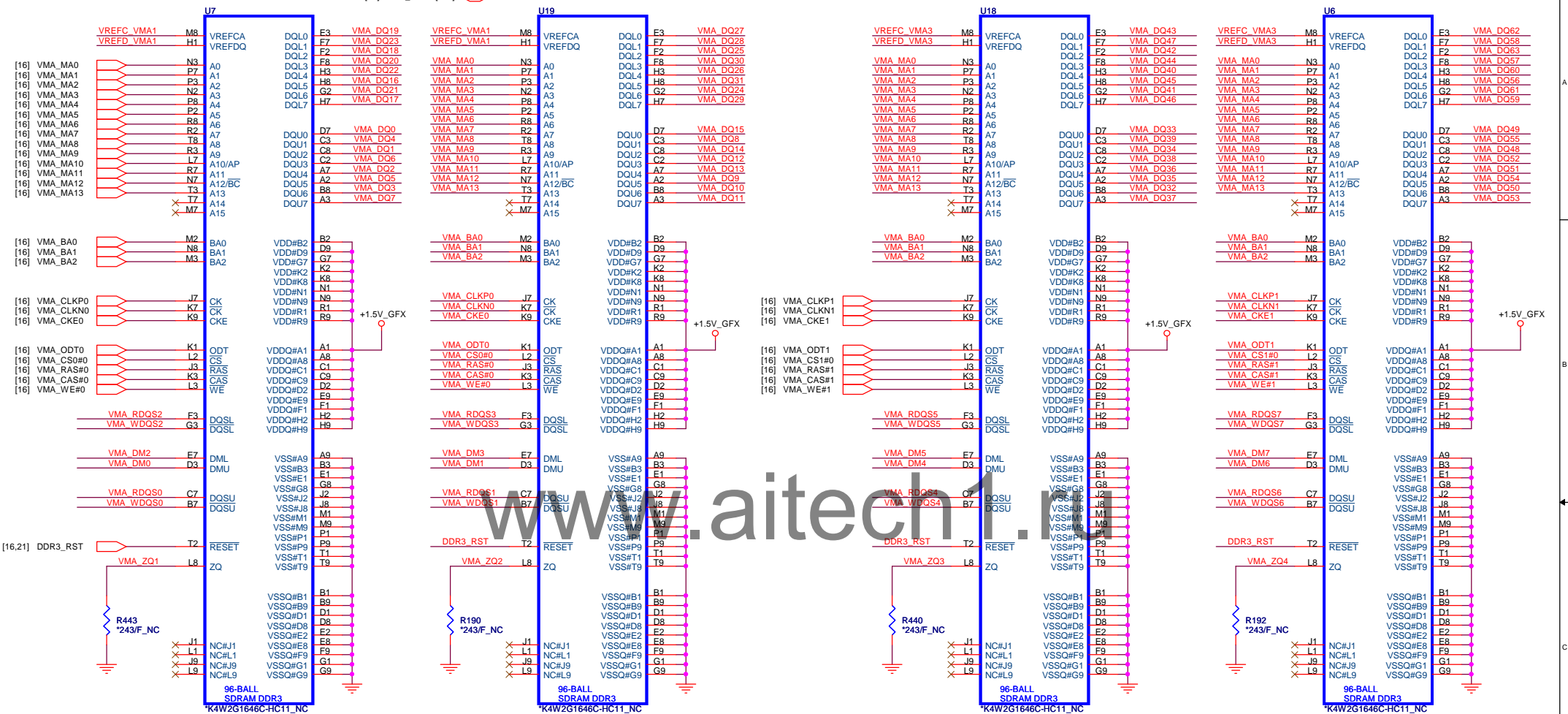
PX\_EN=1, for BACO MODE  
PX\_EN=0, for Normal Operation (Default)

BACO MODE : +BIF\_VDDC ( +1V\_GFX )  
Normal : +BIF\_VDDC ( +VCC\_DGFX )

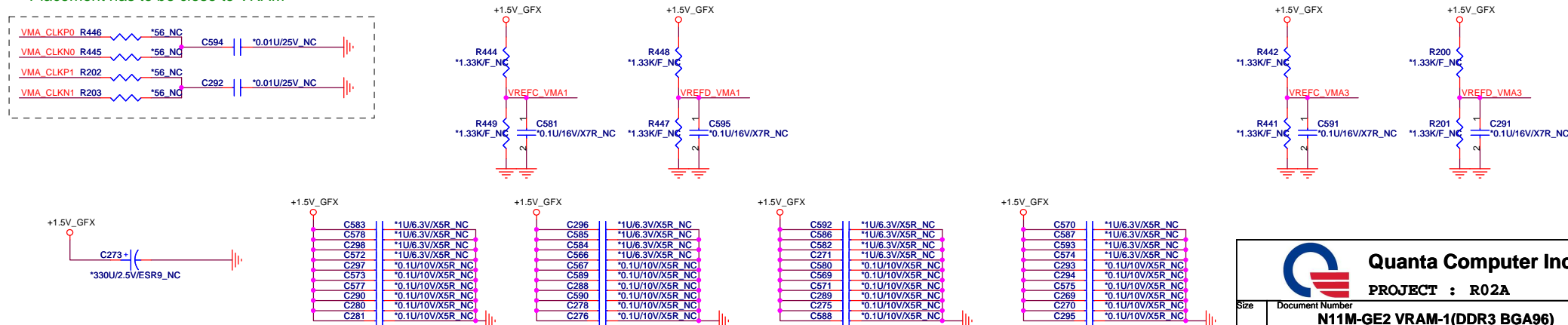
Reserve for support BACO mode

Power sequence control +3V\_GFX>+VCC\_DGFX\_CORE

**CHANNEL A: 1024MB DDR3**



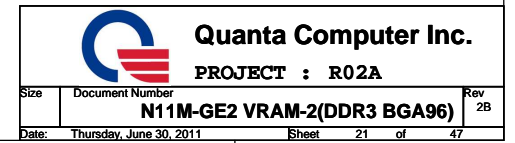
Placement has to be close to VRAM

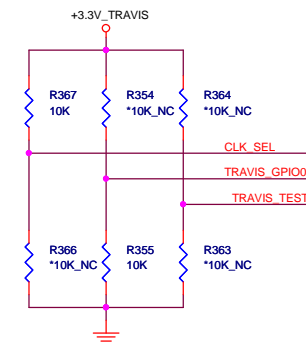
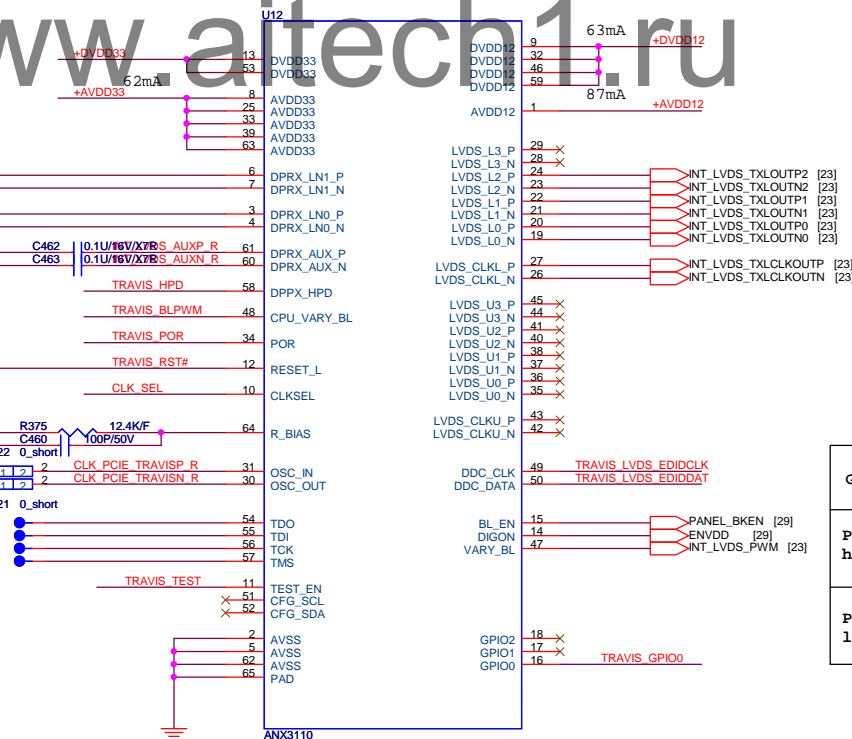
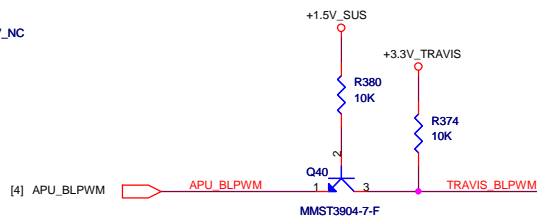
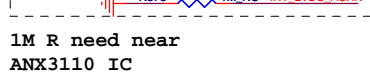
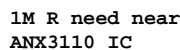
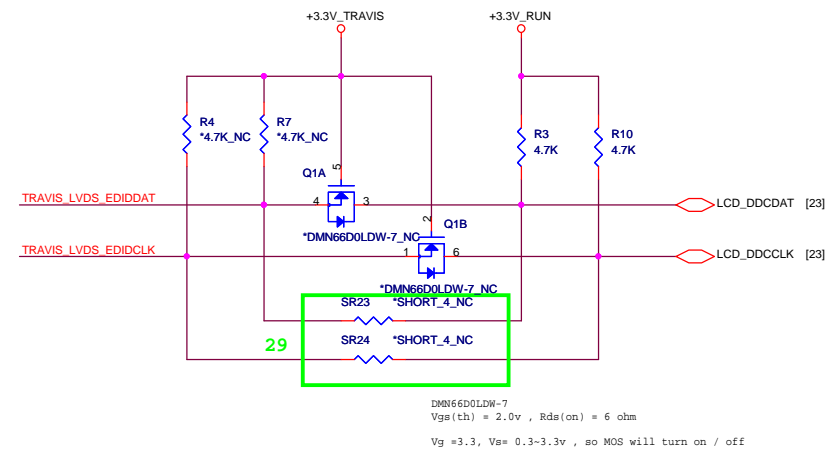


A diagram showing a 4x4 grid of hexagons. The leftmost column of four hexagons is connected by a red line. The rightmost column of four hexagons is connected by a blue line. The four hexagons in the second column from the left are connected by a blue line. The four hexagons in the third column from the left are connected by a blue line.

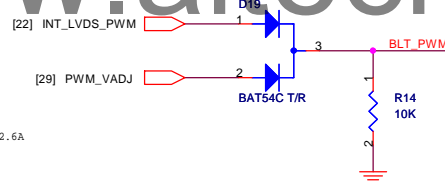
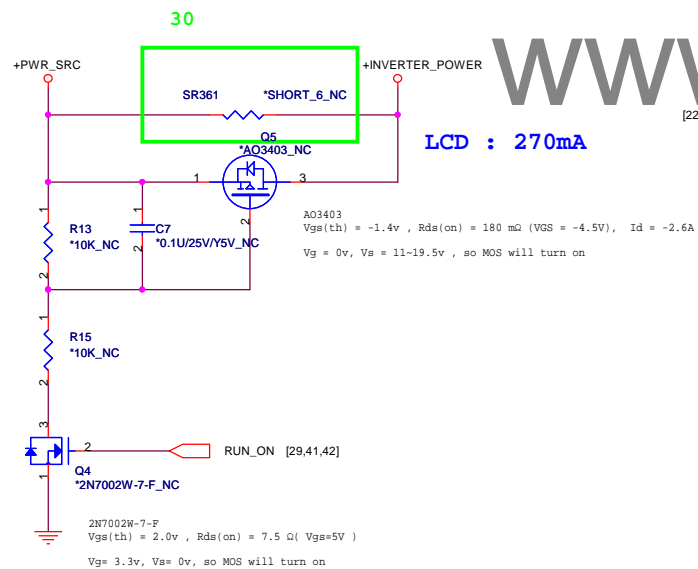
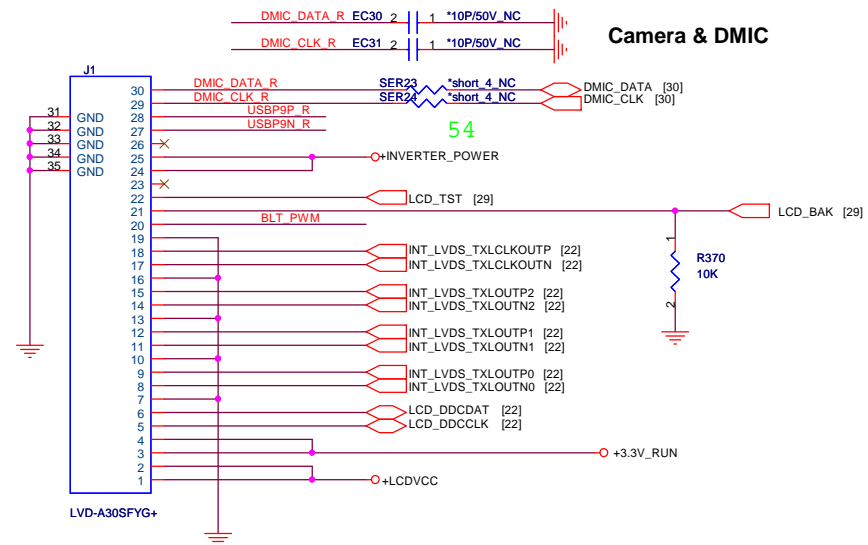
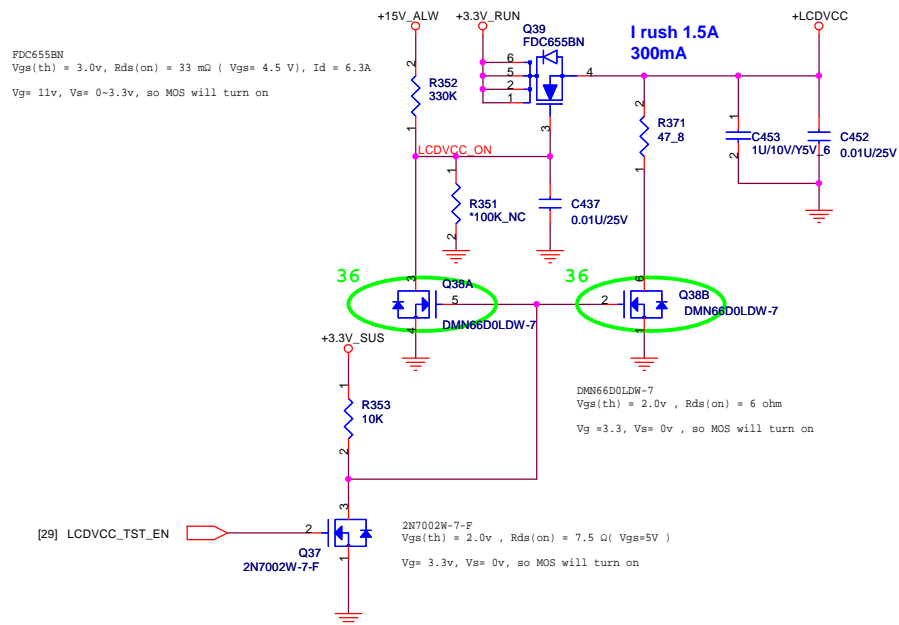


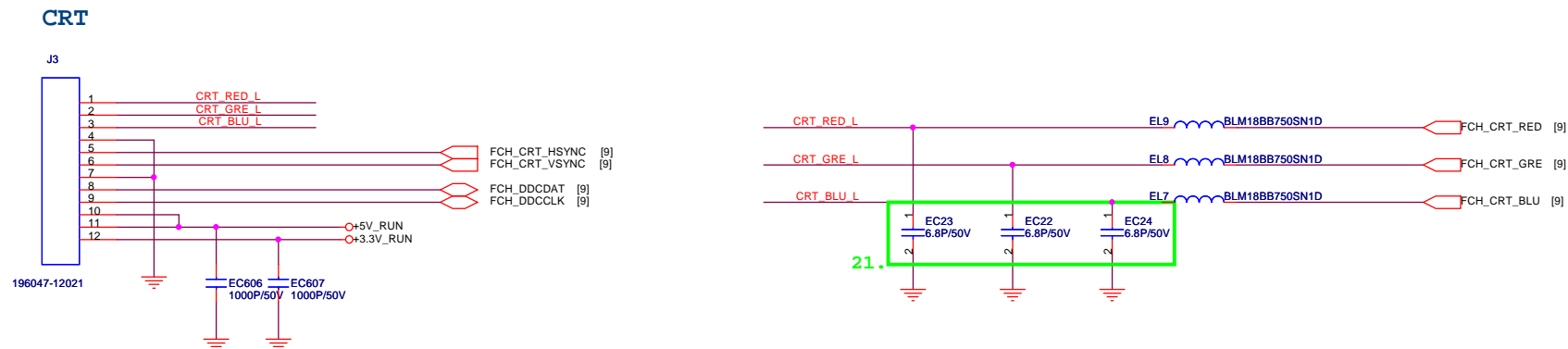
A schematic diagram showing a capacitor labeled C130 with a value of \*22U/6.3V/X5R\_8\_NC. The capacitor is connected between a +1.5V\_GFX supply and a ground symbol.





GPIO	CLK_SEL	TRAVIS _GPIO0	TRAVIS. _TEST
Pull high	differential 100Mhz Setting	Control by HW	TEST mode enable
Pull low	OSC 27Mhz	Control by SW Setting	TEST mode disable Setting

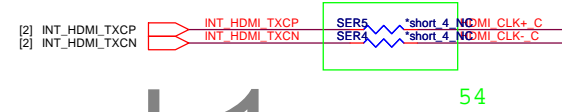
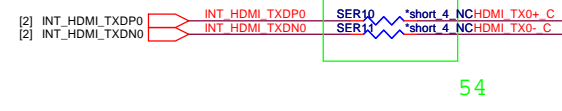
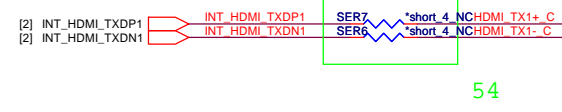
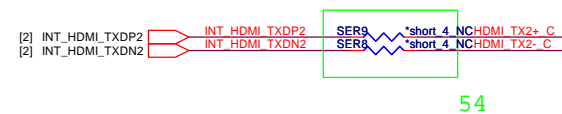
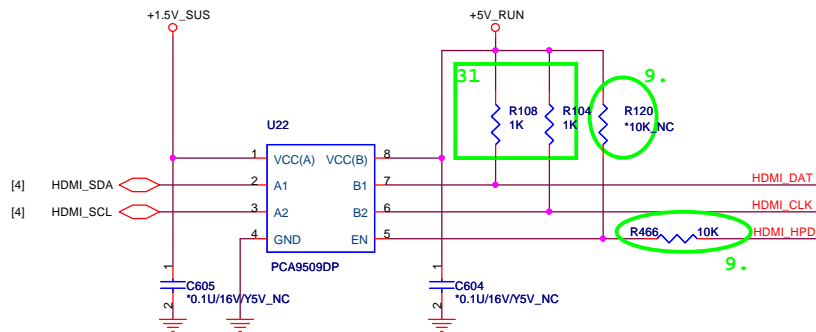




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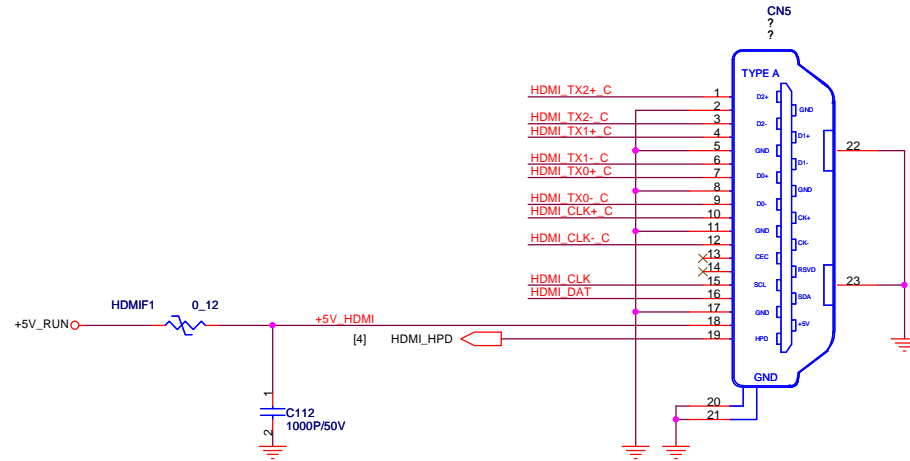
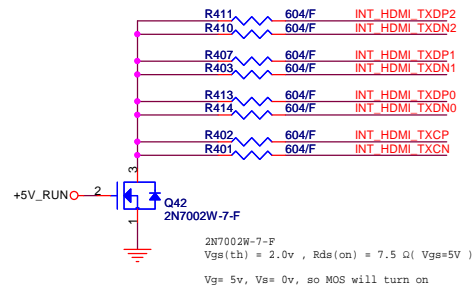
# DIS HDMI

Reserve for EMI and close to HDMI CONN



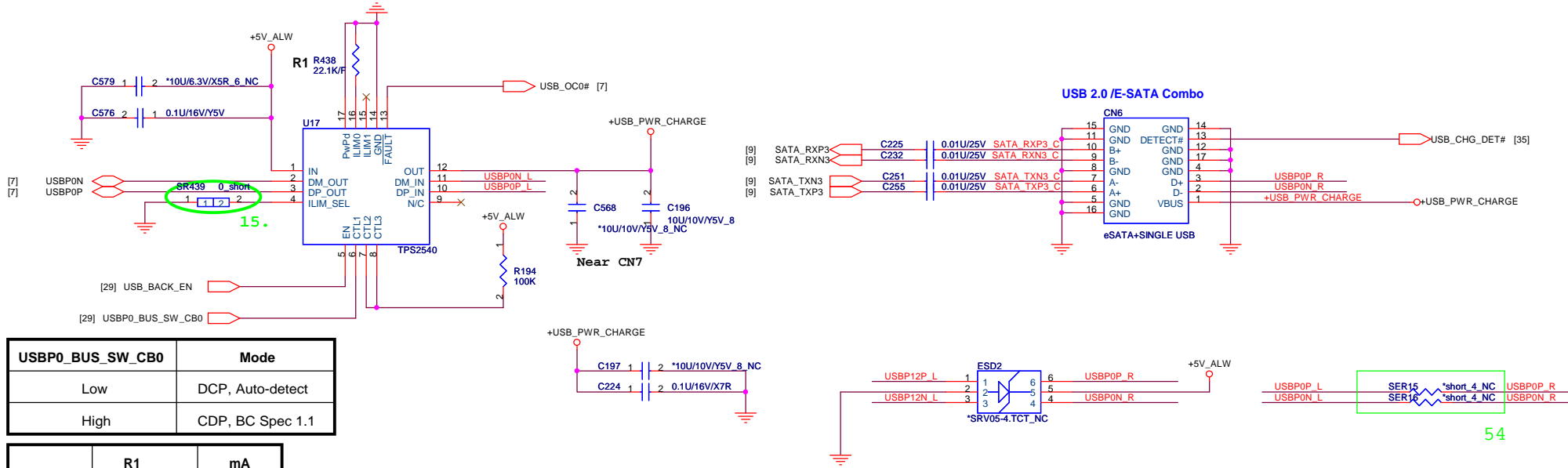
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HDMI Conn.



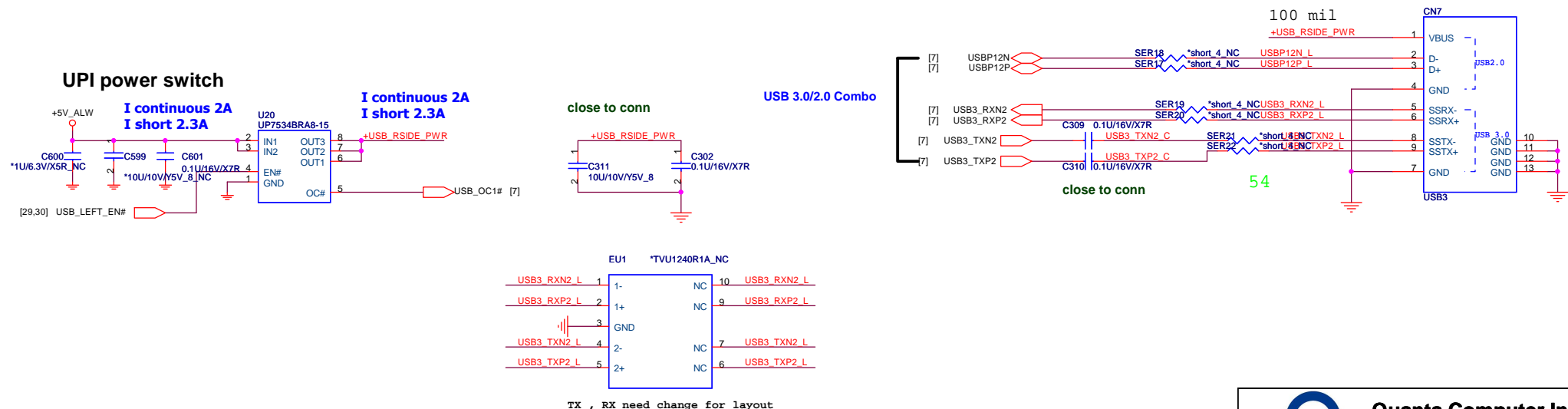
S3/S5 USB charging circuit

USB2.0 + ESATA + USB Conn + Power share

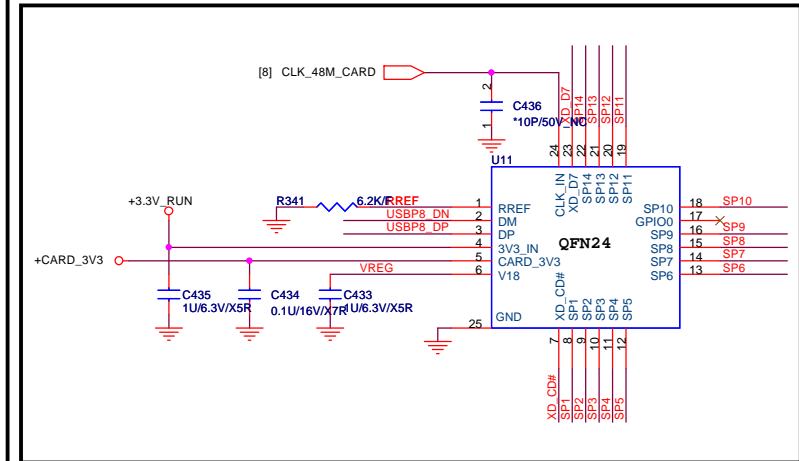
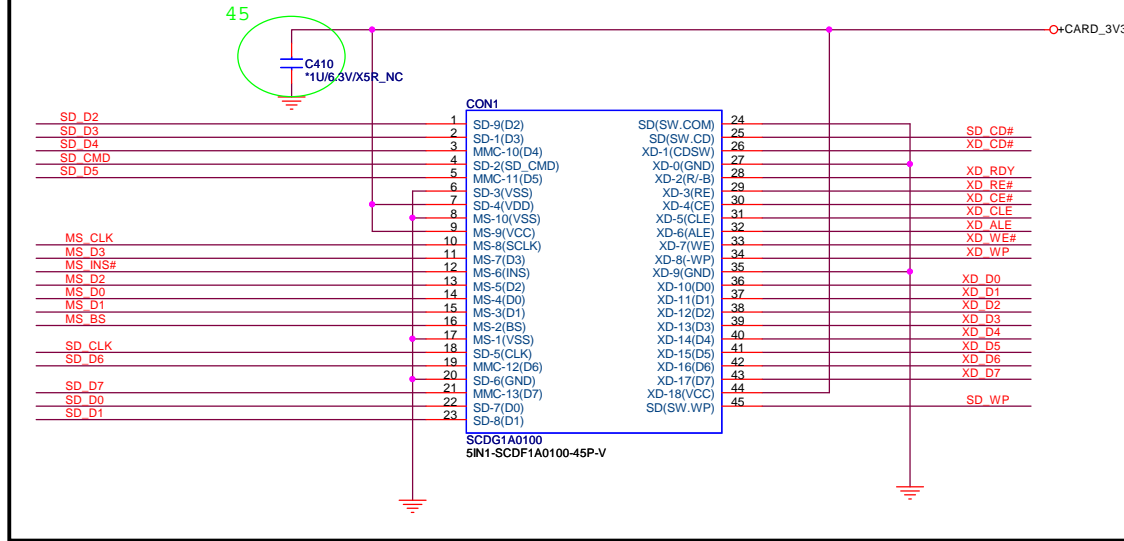


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USB3.0 + USB2.0 + USB Conn



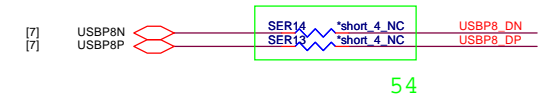
# Inspiron



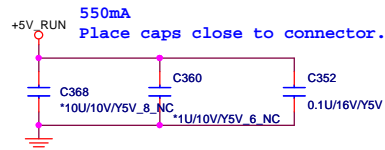
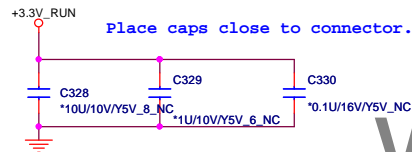
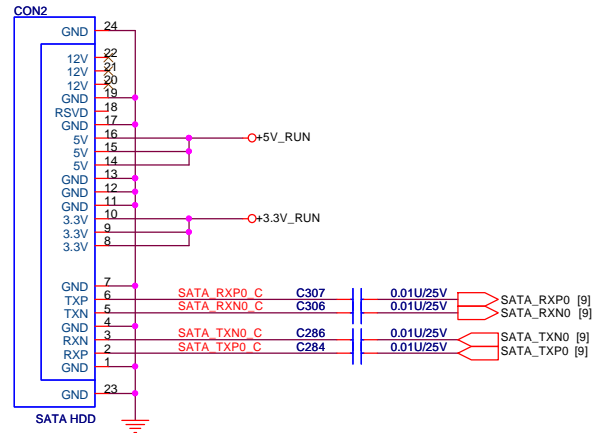
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VOSTOR 3.

SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D7	MS D3
SP5	XD ALE	SD CD#	MS D6
SP6	XD WE#	SD D6	MS D2
SP7	XD WP	SD CLK	MS D0
SP8	XD D0	SD D5	MS D0
SP9	XD D1	SD CMD	MS D4
SP10	XD D2	SD D4	MS D1
SP11	XD D3	SD D3	MS D5
SP12	XD D4	SD D2	MS BS
SP13	XD D5		
SP14	XD D6		

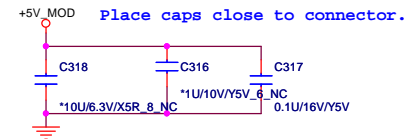
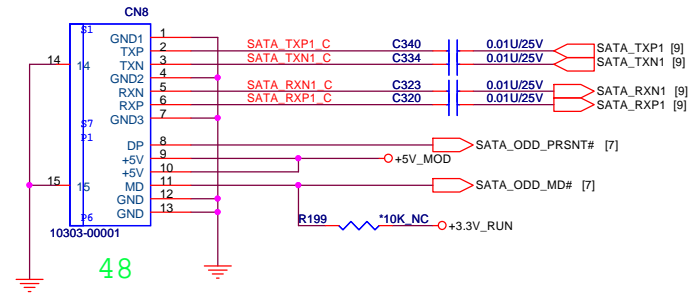
Share Pin



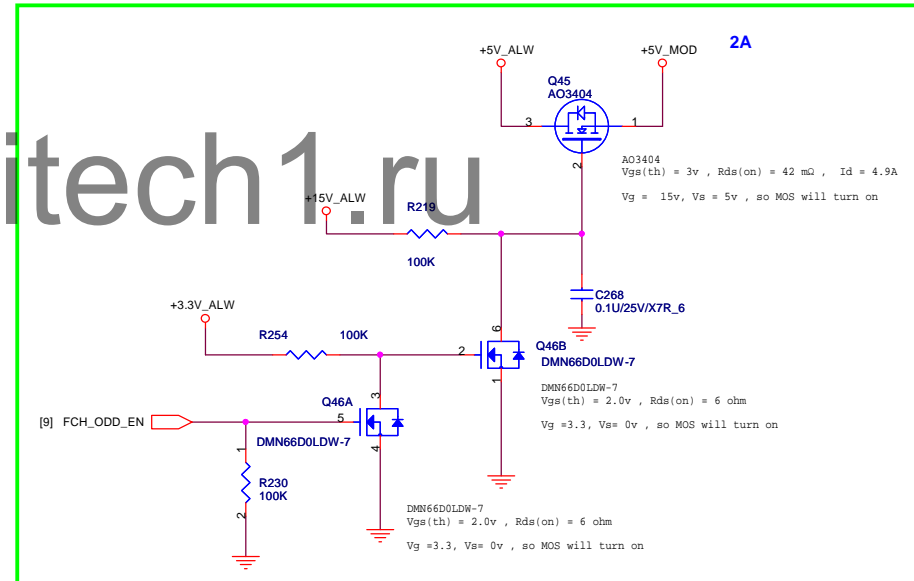
## SATA Connector



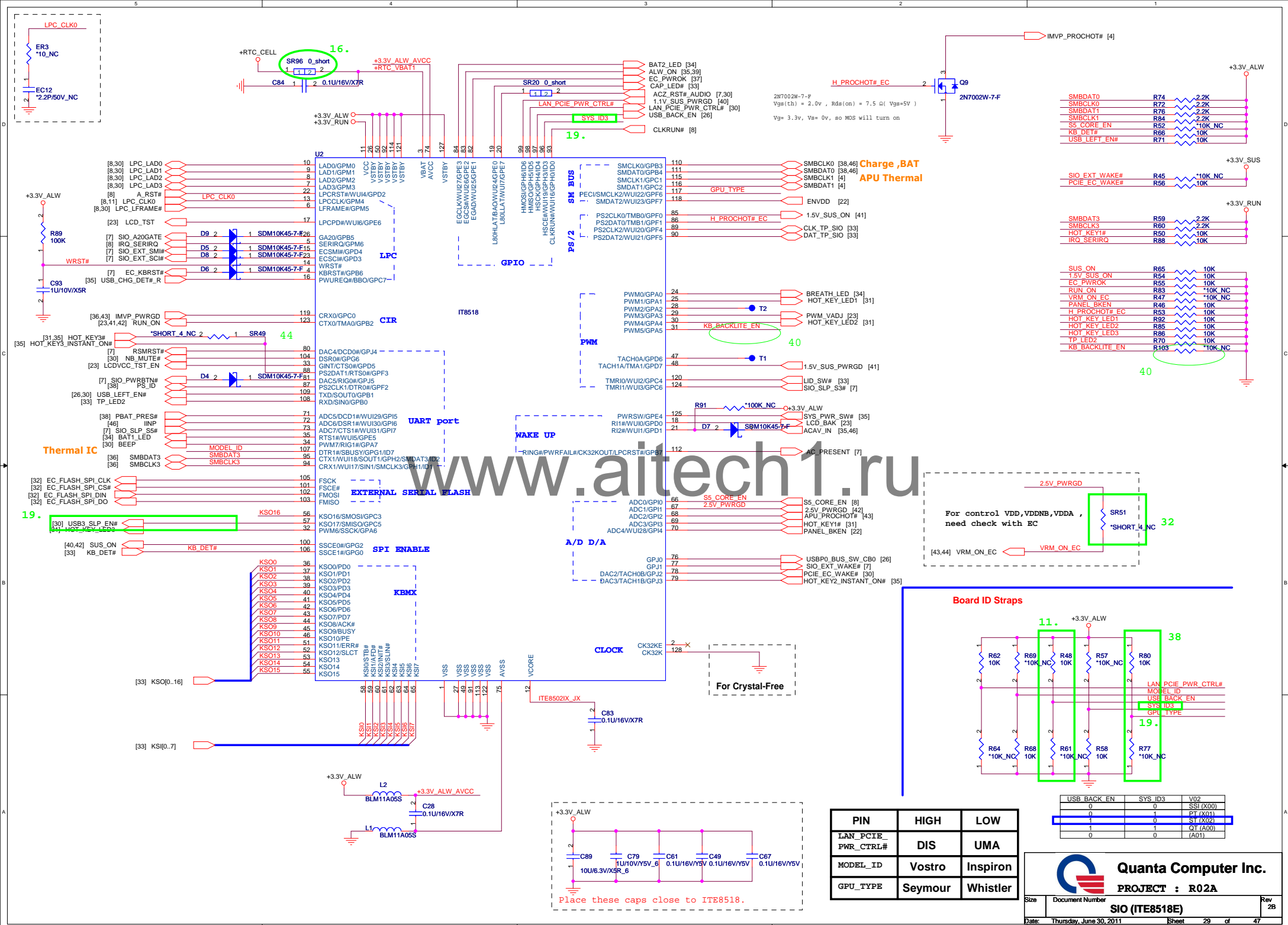
## ODD Connector



5.



40



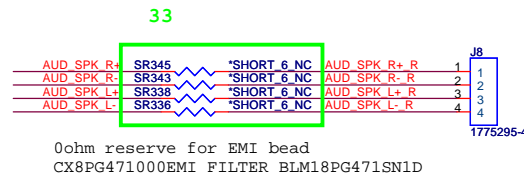
Combo/WLAN

LAN

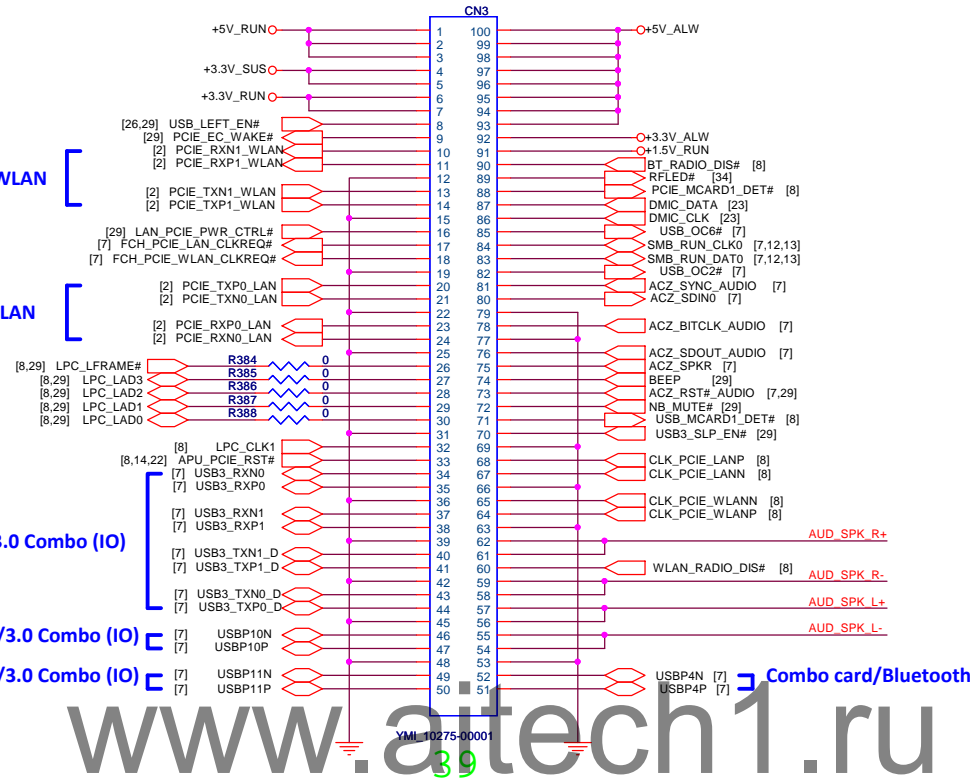
USB2.0/3.0 Combo (IO)

USB2.0/3.0 Combo (IO)

USB2.0/3.0 Combo (IO)



Int. Stereo Speakers  
5V / 4 Ohm / 2W

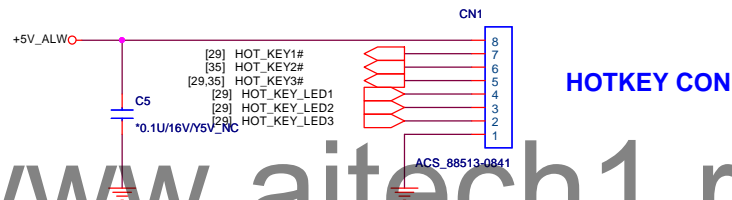


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BTB CONN.

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		2B
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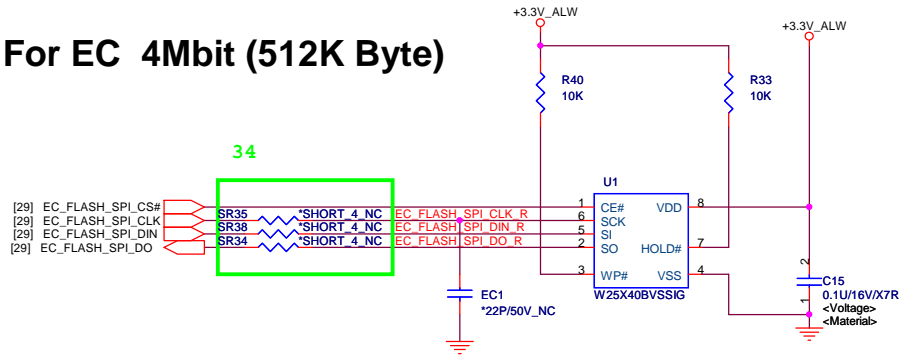


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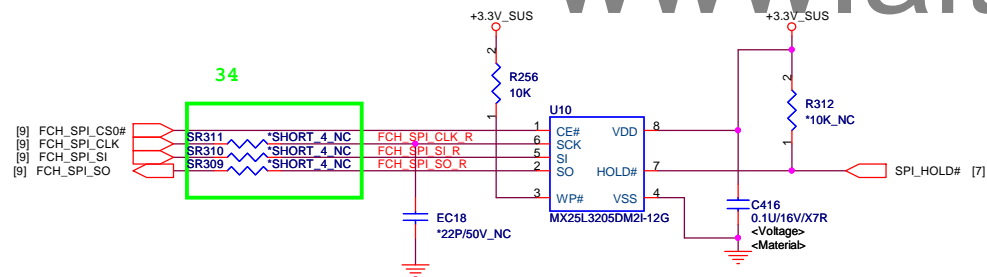
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Size	Document Number	Rev
	<b>HOTKEY CON</b>	2B
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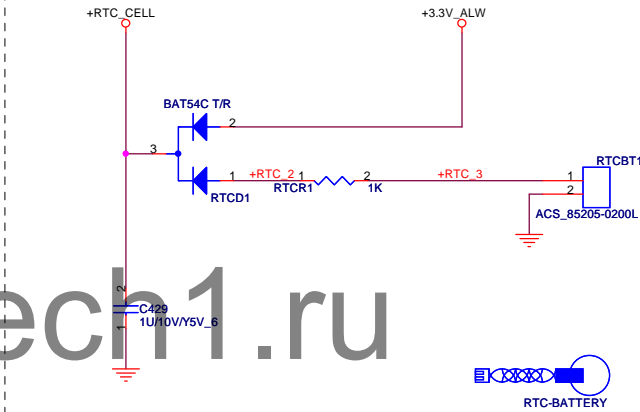
## For EC 4Mbit (512K Byte)



## For FCH 32Mbit (4M Byte)



## RTC



Double, 25'C, Vf=0.4V, If=25mA  
one, 25'C, Vf=0.35V, If=15.8mA

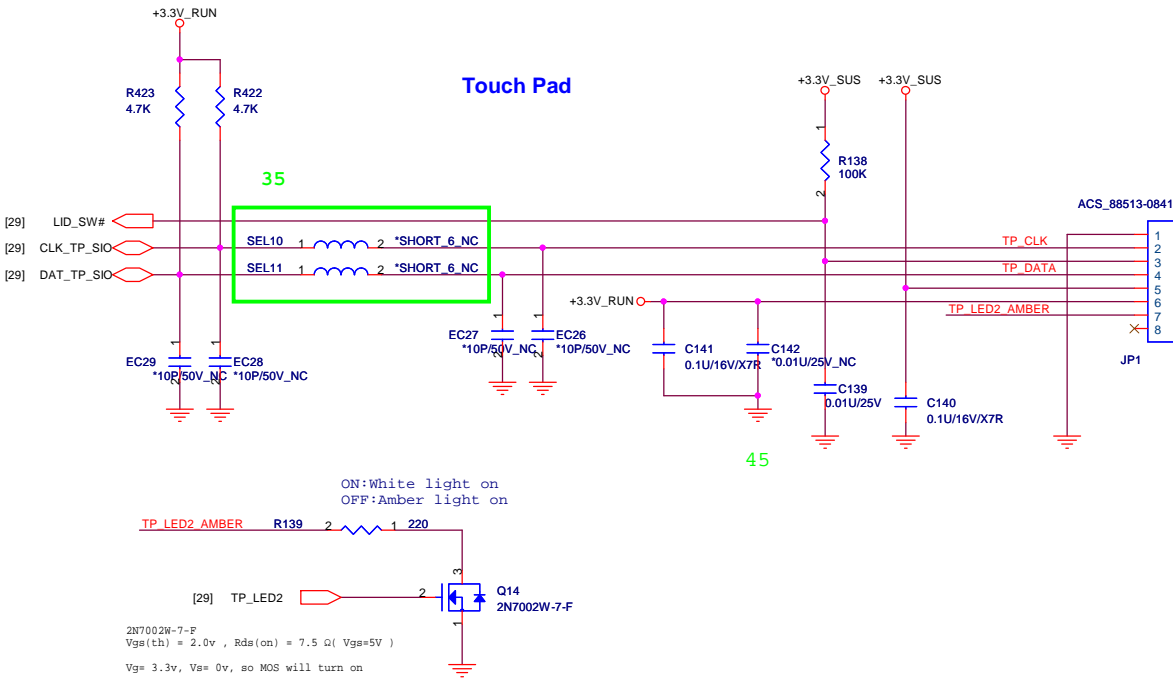


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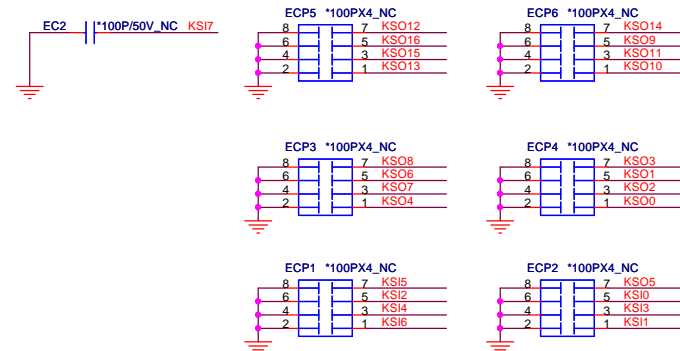
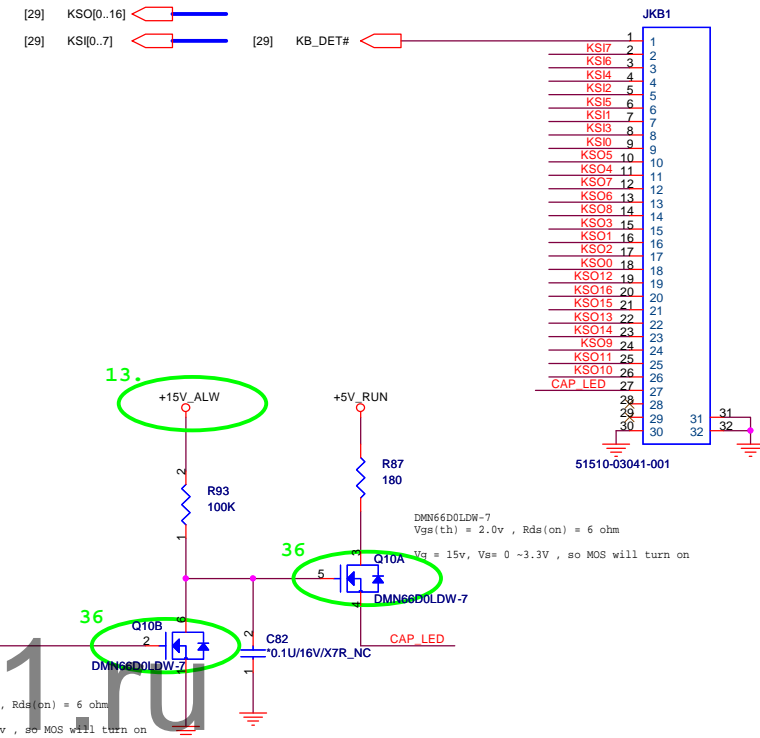
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FLASH / RTC

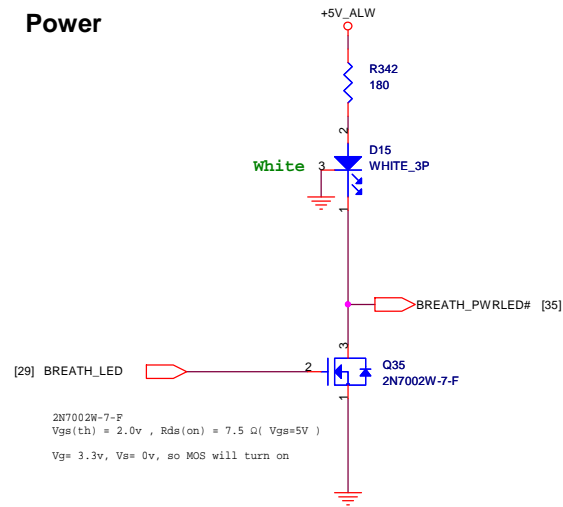


## KEYBOARD CONNECTOR

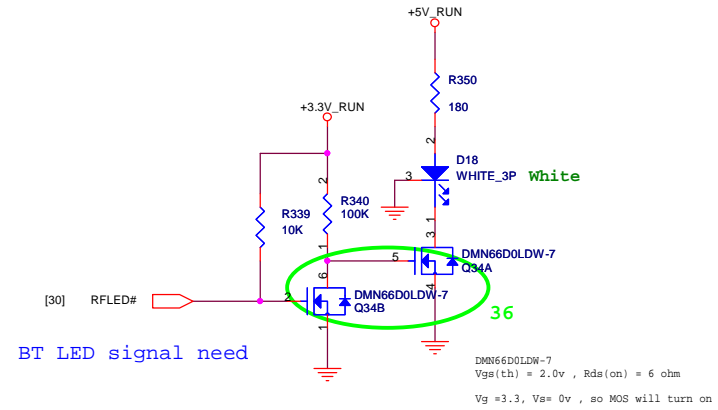


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**PROJECT : R02A**

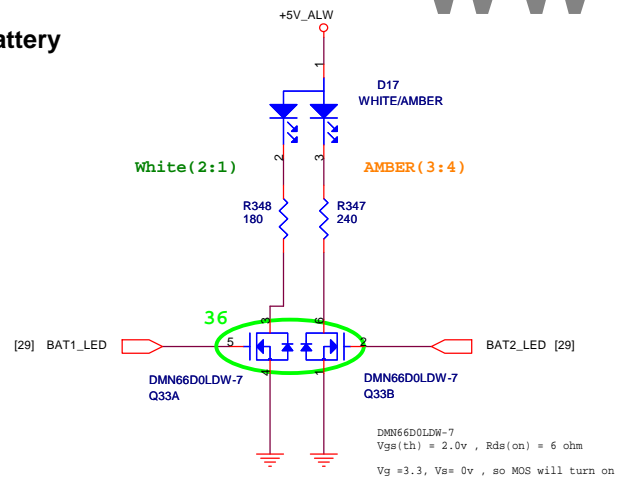
## Power



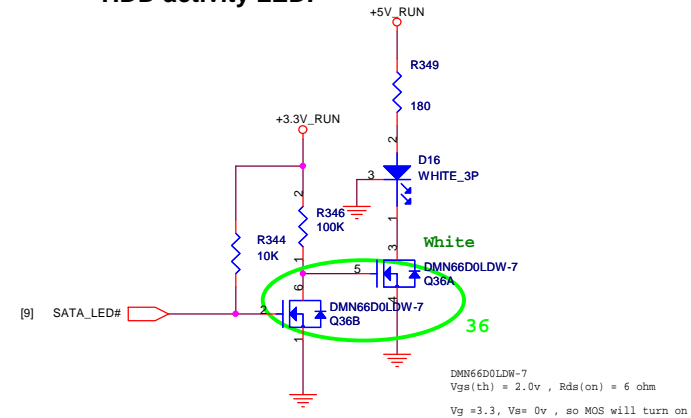
## Bluetooth / WLAN on/off LED



## Battery



## HDD activity LED.



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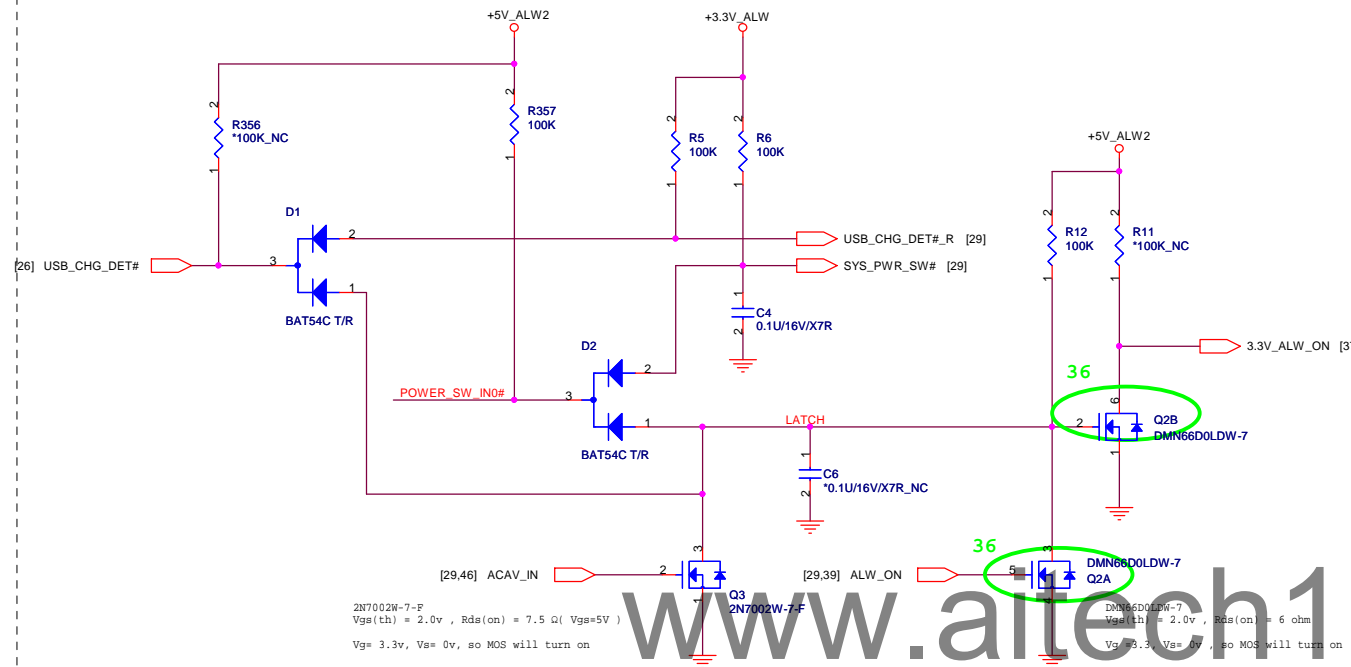


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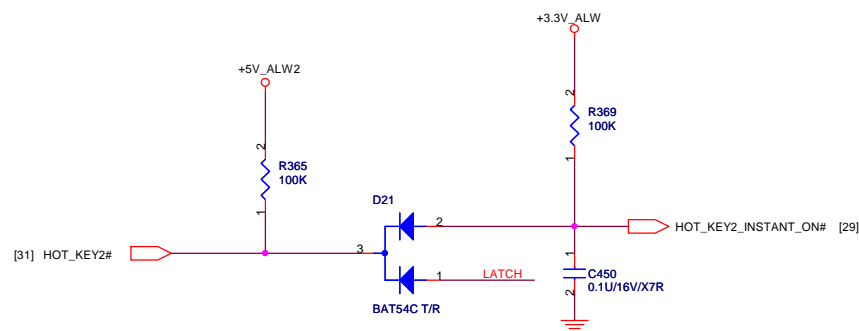
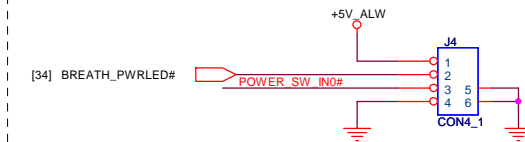
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		2B
Date:	Thursday, June 30, 2011	Sheet 34 of 47

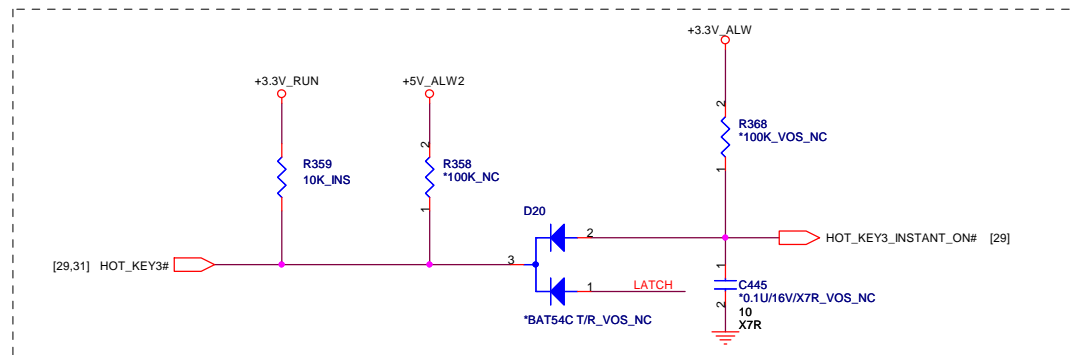
## 3VALW ON POWER LOGIC



## PWR button board



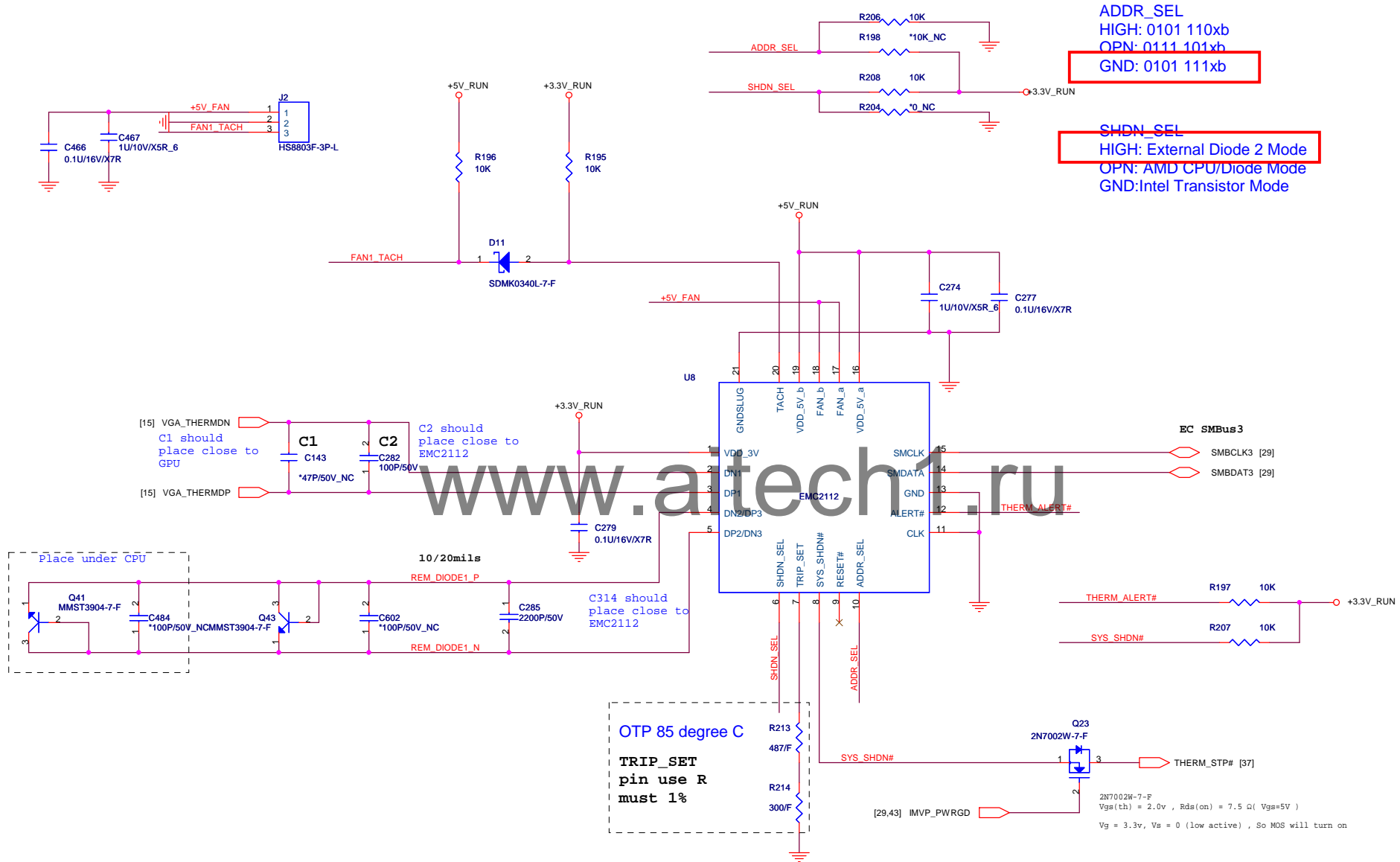
## Instant ON function



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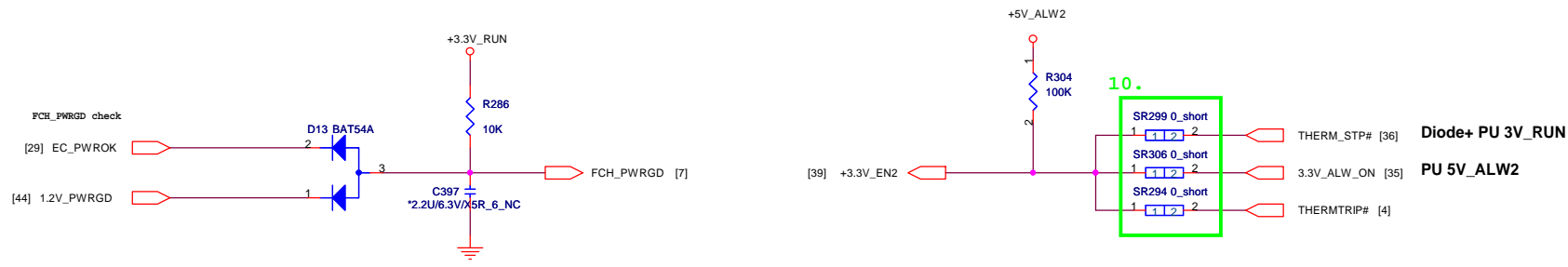
Size	Document Number	Rev
	<b>PWR SW/LED</b>	2B
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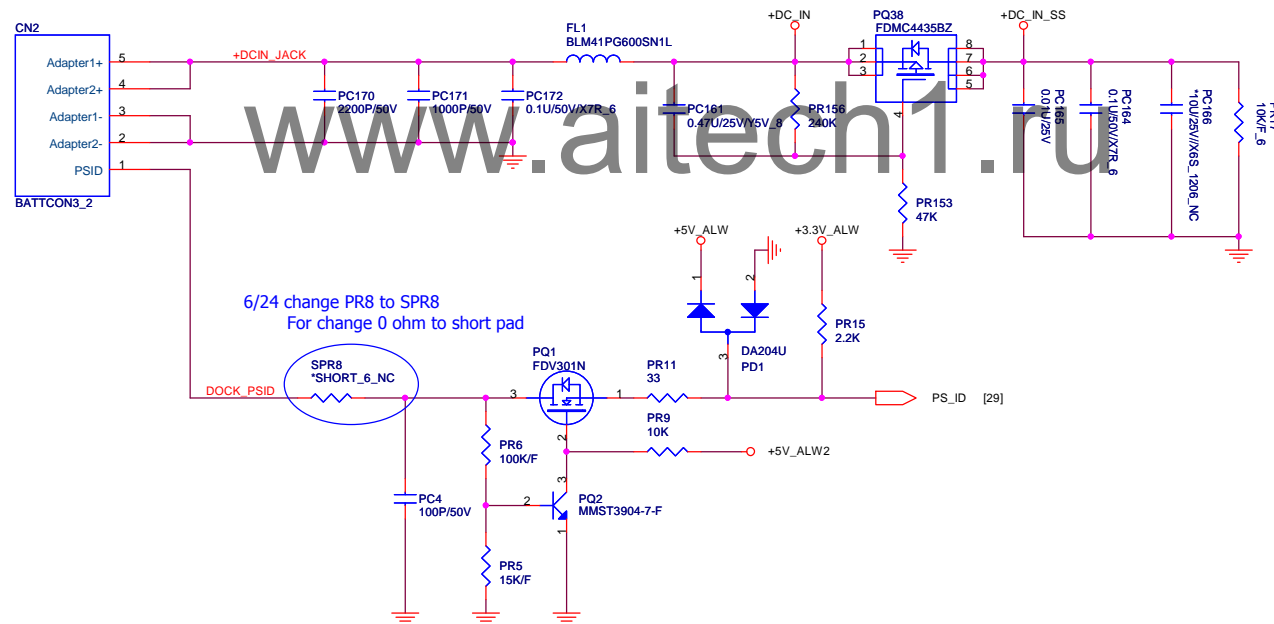
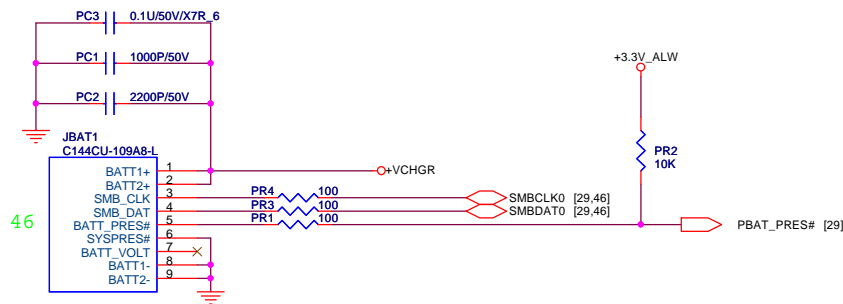
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Size	Document Number	Rev
	<b>FAN &amp; THERMAL</b>	2B
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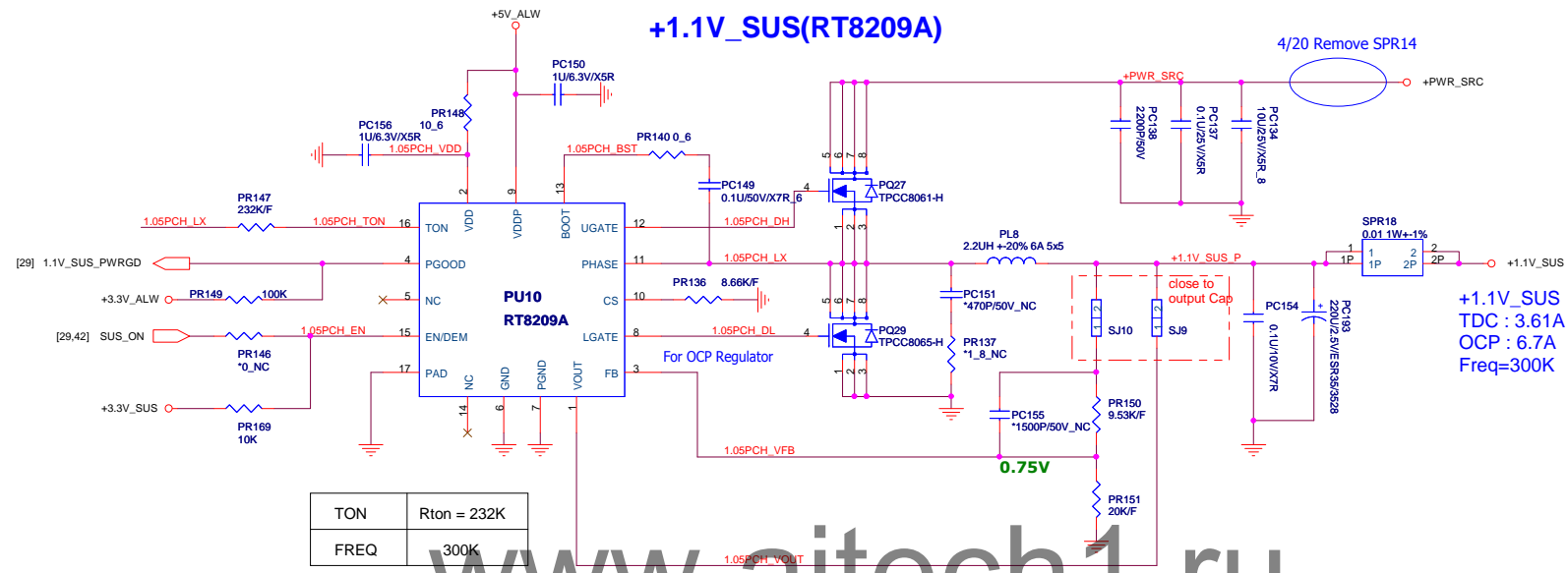


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	<b>DC IN / BATT</b>	2B
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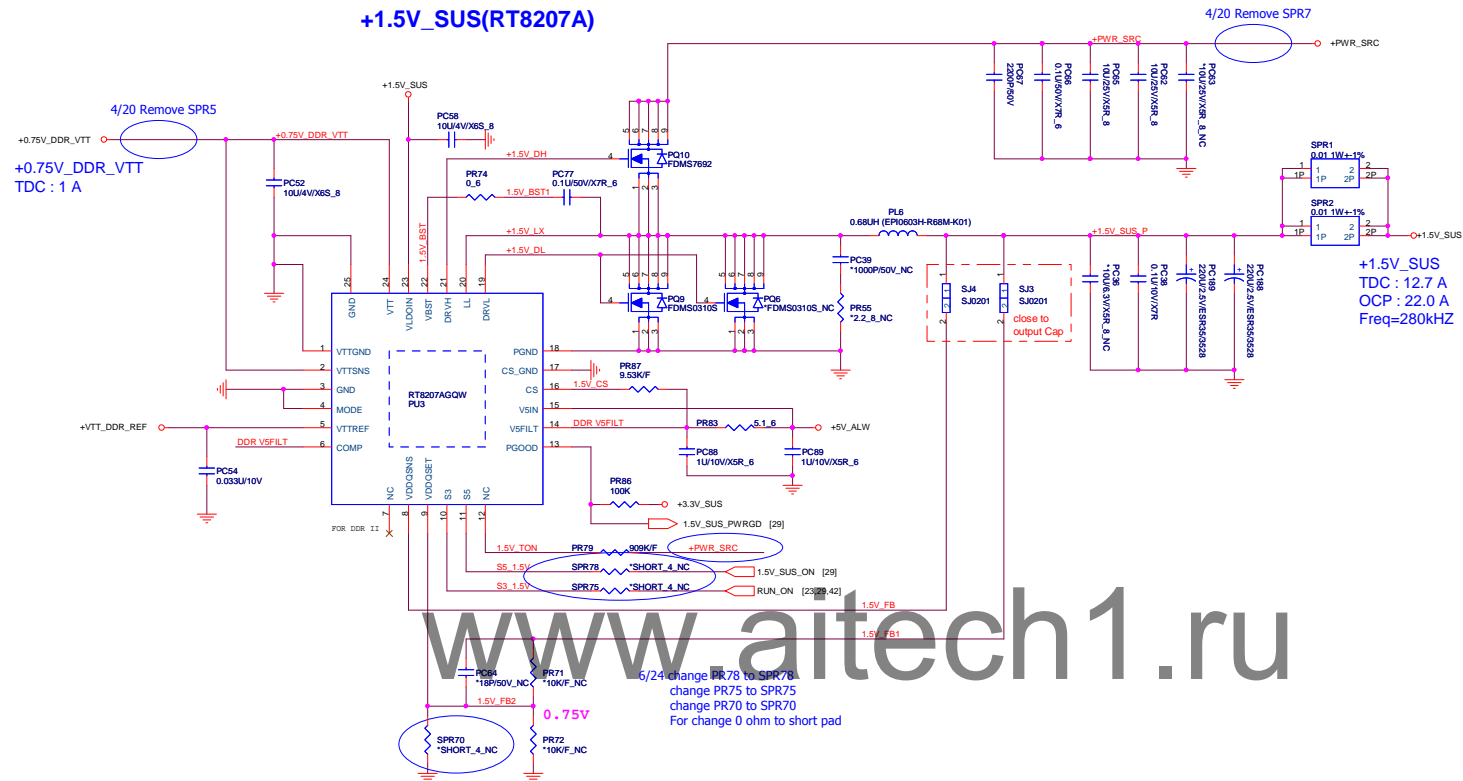
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	<b>+1.1V_SUS (RT8209A)</b>	2B
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VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

